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# CMOS multi-input gate implementations for low-power digital design

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Power consumption is one of the most critical design parameters in analogue and digital circuits. This paper studies different static CMOS implementations of digital logic functions with power and power-delay product as criteria. Two approaches are used. The first one compares the implementation styles by introducing new probabilistic methods in estimating the average power dissipation (dynamic and short-circuit). The second one uses statistics, based on power and delay measurements, to achieve more accurate results. Both approaches indicate the same conclusions in an example of two different implementations of a six-input NAND gate.

## 1. Introduction

In past years most of the research in the area of digital electronics has been directed towards increasing the speed of digital systems. Recently, the increasing demand for portable systems and the moderate improvement in battery performance indicate that the power consumption is one of the most critical design parameters (Chandrakasan *et al.* 1992, 1994, Shimohigashi and Seki 1993, Vittoz 1994).

The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power. Minimizing area and delay has already been considered important, but recently the reduction of the power consumption has been essential. Portability imposes a strict limitation on power dissipation while still demanding high computational speeds. Hence, apart from power consumption, the power-delay product is used as a metric of performance, and this downplays the importance of the area occupied by the circuit.

The reduction of the power consumption requires optimizations at all levels of the design procedure: algorithmic, architectural, logical and layout. In this paper optimization at the logical level is considered. Circuit techniques which are best suited to minimize the power dissipation of a given logic function are examined.

It is well known that one of the main advantages of static CMOS circuits over single-polarity MOS circuits, is that the static power dissipation is very small and limited to leakage (Weste and Eshragian 1992). The power dissipation of a static CMOS gate can be split into two parts $P_D$ (dynamic dissipation) and $P_{SC}$ (short-circuit dissipation). The largest part of the power dissipation caused by charging the output node capacitance ($C_O$), is the dynamic part, given by the equation

$$P_D = V_{DD}^2 C_O a f_g \tag{1}$$

where $V_{DD}$ is the supply voltage, $a$ (activity factor) is the fraction of input transitions in which the steady-state value of the output node changes from logic low to logic

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high, and $f_g$ is the switching frequency of the gate (Chandrakasan *et al.* 1992, Weste and Eshragian 1992, Liu and Svensson 1993). The second part $P_{SC}$ is due to the short-circuit current $I_{SC}$, which arises when a direct path (supply to ground) occurs. For common circuits $P_{SC}$ lies in the range of 5–20% of the dynamic switching component, and is given by the following equation (Weste and Eshragian 1992, Veendrick 1984):

$$P_{SC} = V_{DD} I_{SC} \tag{2}$$

Since most digital CMOS circuitry is composed of simple and/or complex gates, we study the best way to implement logic functions to achieve low power consumption. Furthermore, two new probabilistic approaches in estimating the average power consumption of a circuit are proposed, the first for the average dynamic power dissipation, and the second for the average short-circuit dissipation. Both methods give an estimation of the average power consumption, per input change, and they are useful in comparing various circuit styles or different implementations of the same logic function. The emphasis of this work is on comparing two different implementations for multi-input gates. This is performed theoretically by using the two probabilistic methods, and in a more accurate way using a statistical approach based on power and delay measurements.

In this paper the one-stage implementation of a multi-input gate and its decomposition into simple gates are compared. The rest of the paper is organized as follows. In § 2 theoretical considerations about the estimation of the average power dissipation (dynamic and short-circuit), and their application to the problem of comparing the two different implementations of a multi-input gate are presented. An analytical comparison which uses a statistical approach, based on power and delay measurements for both implementations, and experimental results are given in § 3. Also, in this section a discussion about the results is presented, and in § 4 some conclusions are given.

## 2. Probabilistic methods

It is important after the logical design of a circuit, to have an estimation of the average power consumed by the circuit. Several power estimation approaches have been proposed. These include simulation-based (Kang 1986), probabilistic (Najm 1993, 1994, Devadas *et al.* 1992), and statistical (Burch *et al.* 1993) methods.

In cases where the designer needs a fast estimation of the average power consumption, the probabilistic methods are the most suitable, due to the fact that they overcome the problem of input pattern dependency. The proposed probabilistic approaches of this section, are useful in comparing the average power dissipation of various circuit styles, or various implementations of the same function.

### 2.1. *Proposed methods*

Dynamic dissipation represents the dominant term of the power that is consumed in a static CMOS circuit. We propose as a new metric for the dynamic power dissipation of a circuit the 'average dynamic power dissipation per input change' $P_D$ which is given by the following formula:

$$P_D = \frac{V_{DD}^2}{T} \sum_{i=1}^{n} (C_i P_i) \tag{3}$$

where $V_{DD}$ is the supply voltage, $n$ is the number of circuit nodes (output of gates), $T$ is the worst-case time interval which is needed for a function completion of the circuit, $C_i$ is the total capacitance of the node $i$, and $P_i$ is the fraction of input transitions in which a 0 to 1 transition occurs at node $i$. $P_i$ is calculated using the following equation:

$$P_i(0\rightarrow 1)=P_i(0)P_i(1)=P_i(0)[1-(P_i(0))] \tag{4}$$

where $P_i(0)$ and $P_i(1)$ are the probabilities the steady-state value of the node $i$ to be 0 or 1, respectively.

In calculating the worst-case time interval $T$ which is needed for a function completion of a gate a model which was developed to calculate delays in $RC$ trees is used (Weste and Eshragian 1992, Rubenstein *et al.* 1983). In this model an effective resistance is used for each transistor type (n or p). For a group of $k$ transistors in series, $T$ is given by the following formula:

$$T=\sum_{k} R_k C_k \tag{5}$$

where $R_k$ is the summed resistance from point $k$ to power or ground and $C_k$ is the capacitance at point $k$. Note that (5) must be used for the worst-case path from the output node of a gate to power or ground.

Short-circuit dissipation is the second component of the power consumed by a circuit that it is considered in our analysis. When a direct path from supply to ground exists, it is assumed for simplification that MOS devices are in the linear operating regime, and gates are without load. When a direct path from supply to ground occurs, some devices in both pull-up and pull-down logic of a gate are simultaneously ON (Veendrick 1984, Rouatbi *et al.* 1992). This results in a short circuit current $I_{sci}$ (Fig. 1). The short-circuit dissipation $P_{sci}$ of a gate is estimated by

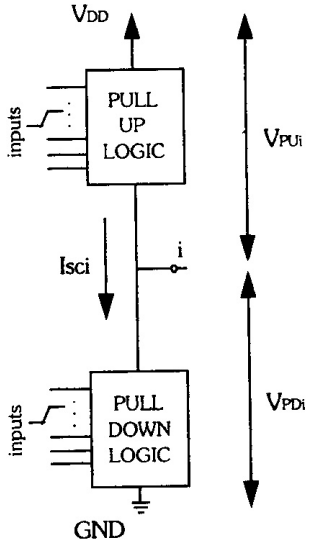


Figure 1. Short-circuit current in a static CMOS gate during inputs switching.

| | |
|---|---|
| Events | E1 = A direct path (supply to ground) occurs at the gate with output $i$<br>E2 = The direct path (supply to ground) is $j$ |
| $P_{ij}$ | $P_{ij} = P(\text{E2/E1})P(\text{E1})$ |

Table 1. Calculation of the $P_{ij}$. $P$(E2/E1) is conditional probability (Miller *et al.* 1990).

$$P_{sci} = V_{DD} I_{sci} = V_{DD}\left(\frac{V_{PUi} + V_{PDi}}{R_{AVGEQi}}\right) = \frac{V_{DD}^2}{R_{AVGEQi}} \tag{6}$$

where

$$\frac{1}{R_{AVGEQi}} = \sum_{j=1}^{m} \frac{P_j}{R_j} \tag{7}$$

In the above equations $R_{AVGEQi}$ represents the 'average equivalent resistance' of the direct path, $m$ is the number of possible direct paths at the gate with output node $i$, $P_j$ is the probability that the $j$ direct path exists, and $R_j$ is the equivalent resistance of the $j$ direct path.

The 'average short-circuit dissipation per input change' is used as a metric to estimate the short-circuit dissipation of a circuit. Since gates are assumed with no loading capacitance, an upper bound (Veendrick 1984) of this metric is given by the following formula:

$$P_{SC} = V_{DD}^2 \sum_{i=1}^{n}\left(\sum_{j=1}^{m} \frac{P_{ij}}{R_{ij}}\right) \tag{8}$$

where $n$ is the number of circuit nodes, $R_{ij}$ is the equivalent resistance of the $j$ direct path of the gate with output node $i$, and $P_{ij}$ is the probability that the $j$ direct path at the gate with the output node $i$ exists. In Table 1 the calculation method of the $P_{ij}$ probability is given. Note that for NAND and NOR gates which are the most widely used in common circuits, the E1 event (Table 1) occurs when a transition from either 0 to 1 or 1 to 0 at the output node of the gate occurs, and in the case where the inputs of the gate change simultaneously.

### 2.2. *Comparison of two implementations*

We have studied two different implementations of a six-input NAND gate. However, our approach can be applied to any multi-input logic gate. In Fig. 2 the one-stage implementation of the six-input NAND gate is shown, and in Fig. 3 its decomposition into simple gates (multiple stage implementation) is illustrated. In both implementations minimum-sized transistors are used in order to reduce the parasitic capacitance. In the following a simple model of the MOS transistor capacitances is used (Weste and Eshragian 1992), with gate capacitance $C_g$, in addition to all capacitances associated with the drain of the device (such as diffusion, sidewall and overlap capacitance) $C_d$. It is reasonable to assume that $C_g \cong 4{\cdot}5C_d$.

Each implementation is assumed to be loaded with the same load capacitance: $C_L = 2C_g$ in the calculation of the average dynamic power dissipation per input change. Using the above MOS transistor capacitances, which are noted in Figs 2 and

3, the total capacitance of each node for the two implementations is calculated. In the case of parallel connected transistors the drain capacitances of each transistor pair (connected to the output of a gate) are merged. For instance in a six-input NAND gate (see Fig. 2) the total capacitance associated with the drains of the six parallel connected p-type transistors is equal to $3C_d$ (not $6C_d$). From (4) the power consuming transition (0 to 1) probabilities at the nodes of both implementations are calculated. The worst-case time interval $T$ which is needed for a function completion of the two implementations is computed using (5). In this computation is assumed that the ratio of the effective resistances for the n- and p-type transistors is $R_p/R_n \cong 2{\cdot}5$. Also, a time constant $\tau = R_n C_g$ is used. The results are shown in Table 2.

In order to have a realistic comparison of the average dynamic power dissipation per input change between the two implementations, we consider in both cases as the worst-case time interval $T$ for a function completion the larger one ($T = 29\tau$). Using (3) and the data of Table 2 the average dynamic dissipation per input change of the one-stage implementation is given by

$$P_D = \frac{0{\cdot}0444 C_g V_{DD}^2}{29\tau} \tag{9}$$

and for the multiple-stage implementation by

$$P'_D = \frac{1{\cdot}4536 C_g V_{DD}^2}{29\tau} \tag{10}$$

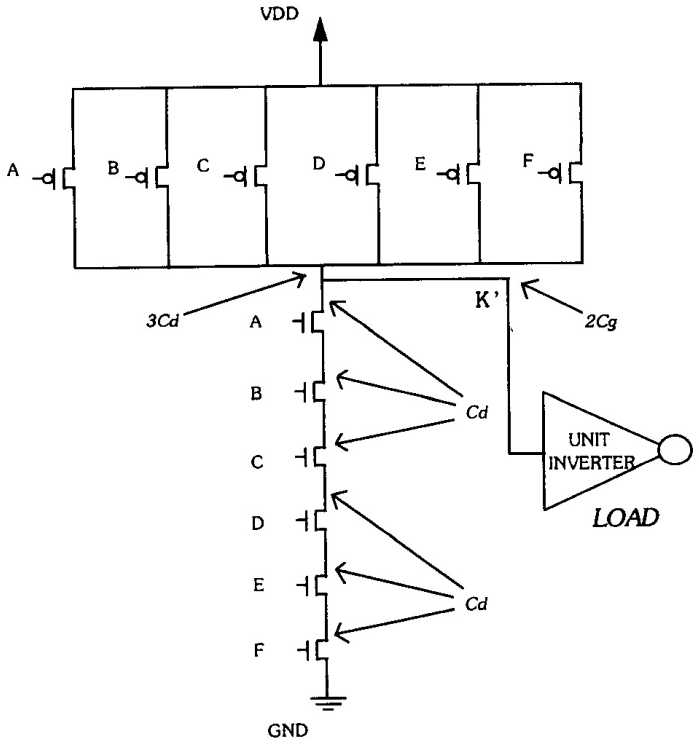


Figure 2. One-stage implementation of six-input NAND gate.

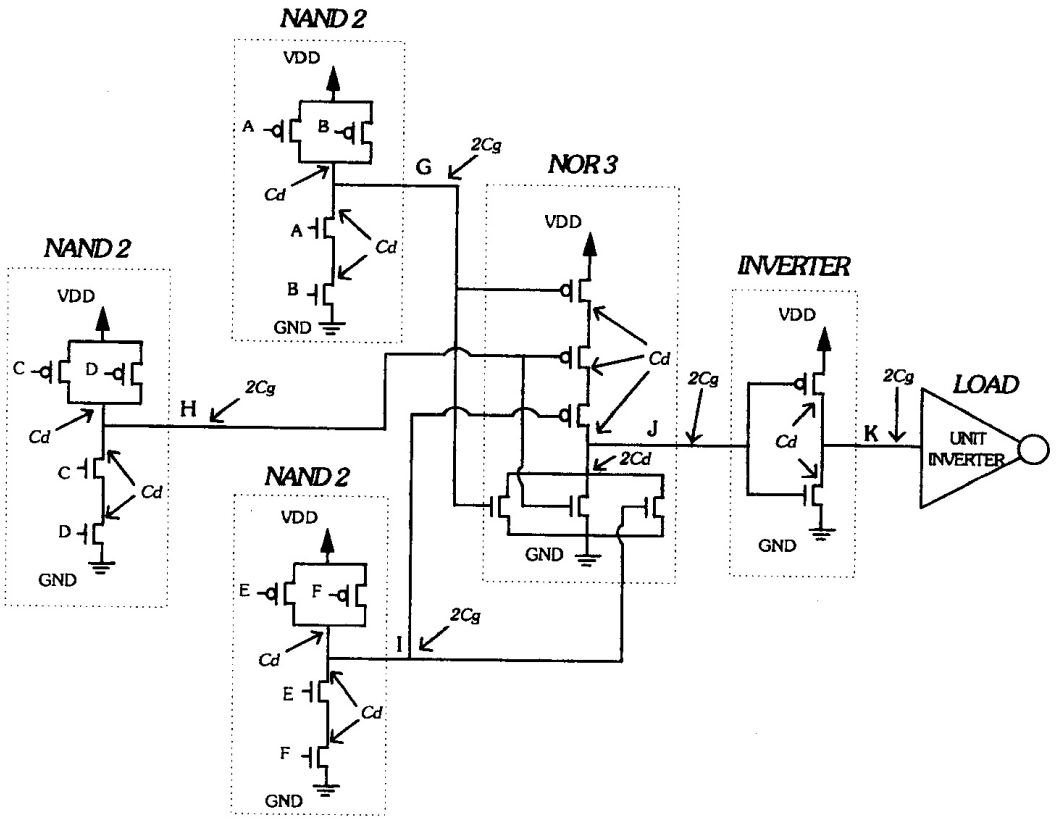


Figure 3. Multiple-stage implementation of six-input NAND gate.

The average dynamic power dissipation per input change ratio of the two implementations is

$$r = \frac{P_D}{P'_D} = 0{\cdot}0305 \tag{11}$$

This means that the dynamic power consumed by the one-stage implementation is less than that of the multiple-stage implementation. The power–delay product ratio which is equal to 0·0217 is smaller than the result in (11), because of the higher speed of the one-stage implementation.

| | One-stage NAND-6 | Multiple-stage NAND-6 | | | | |
|---|---|---|---|---|---|---|
| Nodes | $K'$ | G | H | I | J | K |
| $P_i$ | 63/4096 | 3/16 | 3/16 | 3/16 | 63/496 | 63/4096 |
| $C_i$ | $2C_g+4C_d$ | $2C_g+2C_d$ | $2C_g+2C_d$ | $2C_g+2C_d$ | $2C_g+3C_d$ | $2C_g+2C_d$ |
| $T$ | 20·67$\tau$ | | | 29$\tau$ | | |

Table 2. $P_i$, $C_i$ and T of the two implementations.

| No. of ON parallel transistors | One-stage NAND-6 | Multiple-stage NAND-6 | | | | |
|---|---|---|---|---|---|---|
| | K' | G | H | I | J | K |
| 1 | 12/4096 | 4/16 | 4/16 | 4/16 | 18/4096 | 126/4096 |
| 2 | 30/4096 | 4/16 | 4/16 | 4/16 | 54/4096 | |
| 3 | 40/4096 | | | | 216/4096 | |
| 4 | 30/4096 | | | | | |
| 5 | 12/4096 | | | | | |
| 6 | 64/4096 | | | | | |

Table 3. $P_{ij}$ probabilities for both implementations.

In the following the average short-circuit dissipation per input change of both implementations is computed using (8). In Table 3 the $P_{ij}$ probabilities for the nodes of the two implementations are shown. Also, in Table 4 the equivalent resistance of the possible direct paths of each gate, are given for both implementations. The first columns of these tables show the number of parallel connected transistors which are ON when a direct path (supply to ground) occurs at each gate. This has been carried out because the possible direct path is determined by the number of parallel connected transistors which are ON when a direct path occurs at the gate. For the calculation of the equivalent resistance of the possible direct path, PMOS devices are assumed with an equivalent resistance $R_p$, whereas NMOS devices are assumed with an equivalent resistance $R_n$.

Using (8) the data of Tables 3 and 4 and the ratio of $R_p$ to $R_n$ (which is approximately equal to 2·5) the average short-circuit dissipation per input change of the one-stage implementation is given by

$$P_{SC} = 6{\cdot}7 \times 10^{-3} \frac{V_{DD}^2}{R_n} \tag{12}$$

and for the multiple-stage implementation by

| No. of ON parallel transistors | One-stage NAND-6 | Multiple-stage NAND-6 | | | | |
|---|---|---|---|---|---|---|
| | K' | G | H | I | J | K |
| 1 | $R_p+6R_n$ | $R_p+2R_n$ | $R_p+2R_n$ | $R_p+2R_n$ | $3R_p+R_n$ | $R_p+R_n$ |
| 2 | $(R_p)/2+6R_n$ | $(R_p)/2+2R_n$ | $(R_p)/2+2R_n$ | $(R_p)/2+2R_n$ | $3R_p+(R_n)2$ | |
| 3 | $(R_p)/3+6R_n$ | | | | $3R_p+(R_n)/3$ | |
| 4 | $(R_p)/4+6R_n$ | | | | | |
| 5 | $(R_p)/5+6R_n$ | | | | | |
| 6 | $(R_p)/6+6R_n$ | | | | | |

Table 4. Equivalent resistance $R_{ij}$ of all the possible direct paths.

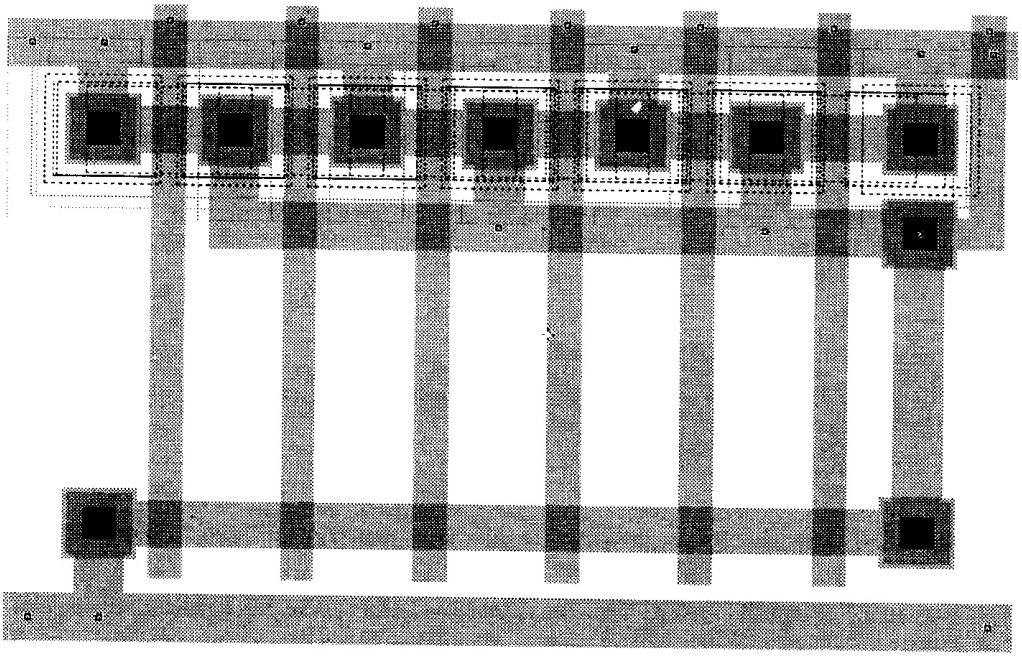

Figure 4. Layout of the one-stage six-input NAND implementation.

$$P'_{SC} = 0{\cdot}41 \frac{V_{DD}^2}{R_n} \tag{13}$$

The results (12) and (13) give an upper bound of the average short-circuit dissipation per input change, since gates with no loading capacitance have been assumed. However, these results can be used as a metric for the comparison of the two implementations in terms of short-circuit dissipation, since they are not far from results when small load is considered (Veendrick 1984). The ratio of the average short-circuit dissipation per unit change of the one-stage implementation to that of the multiple-stage implementation is 0·016. This means that the short-circuit power consumed by the one-stage implementation is less than that of the multiple-stage implementation.

## 3. Statistical approach

The layouts of the two implementations presented in §2.1 were designed in a full-custom manner, using a 1·5 $\mu$m CMOS low-voltage technology. In Figs 4 and 5 the derived layouts are shown and in Table 5 some of their features are listed. In these layouts minimum-sized transistors ($L = 1{\cdot}6\,\mu$m, $W = 2{\cdot}4\,\mu$m) were used. From the layouts circuit equivalents were extracted for a detailed circuit simulation using HSPICE v. H93 (Meta-Software 1992) to obtain the power and delay measures. The transistor parameters used were SPICE level 3 parameters from a 1·5 $\mu$m CMOS low-voltage process, and the simulations were carried out at 27°C, with a supply voltage of 1·5 V. All measurements were obtained with each input supplied through a driver consisting of two minimum-sized inverters in series, and each output node driving a minimum-sized inverter load.

The estimation of power dissipation of a circuit is a difficult problem and has received a lot of attention (Najm 1994, Burch *et al.* 1993, Liu and Svensson 1994,

Kang 1986, Devadas *et al.* 1992). HSPICE can measure the average power consumed by a circuit given a set of input changes, for the time needed for the completion of the internal and output nodes transitions. However, the power dissipation is a strong function of the inputs; thus circuit simulation based techniques for power estimation are expensive in terms of time (Najm 1994, Kang 1986). Several power estimation approaches have been proposed, where possibilities are used to solve the pattern-dependence problem. However, to achieve good accuracy, the spatial and temporal correlations between internal nodes should be modelled, but this can be very difficult (Najm 1993, 1994, Devadas *et al.* 1992). Hence, a statistical approach that combines the accuracy of simulation-based techniques with the speed of probabilistic techniques is followed (Burch *et al.* 1993). In this method the inputs are randomly generated and statistical mean estimation techniques are used to determine the final result. A key point of this technique is the selection of the input patterns to be applied in the simulations. In our example the 63 samples of input changes, which result in a power consuming transition (low to high) at the output node in both implementations, were selected. This selection was made because the one-stage implementation consumes dynamic power, only for these 63 input changes (see §2.2). For the rest of the samples, the multiple-stage implementation consumes power due to the power-consuming transitions at the internal nodes. After the sample selection, each implementation was simulated with the 63 independent, pseudo-random input transitions and the power consumed was monitored. The power dissipation measures do not include the power consumed by the drivers and the loads.

In Figs 6 and 7 the probability distribution of the power dissipation and the power–delay product derived from the measurements, for both implementations of the six-input NAND gate, are shown. As we can see in Fig. 6, the power consumption of the one-stage implementation can be approximated to normal distribution (Burch *et al.* 1993). Hence, the mean power dissipation of the gate is given by

$$\bar{P} \pm t_{a/2} \frac{s}{\sqrt{N}} \tag{14}$$

where $\bar{P}$ is the sample average, $s$ is the sample standard deviation, $N$ is the number of samples, and $t_{a/2}$ is obtained from the $t$-distribution for a $(1-a)\%$ confidence interval (Miller *et al.* 1990). The same result can be extracted from the probability

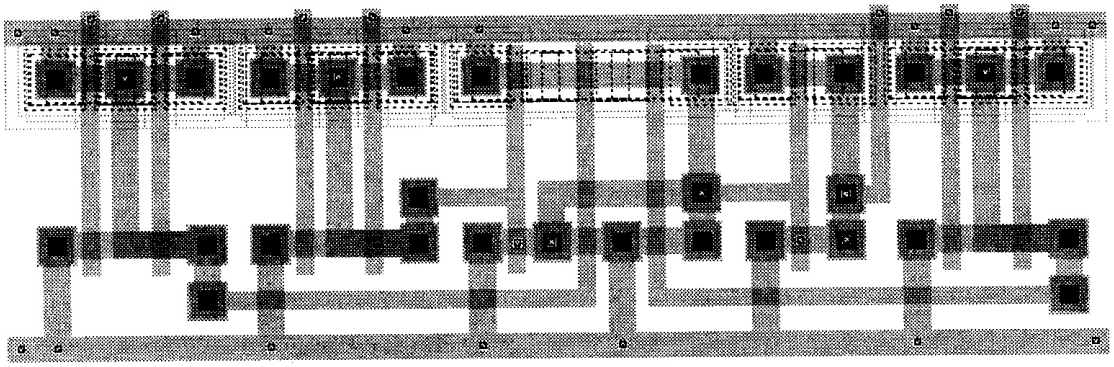

Figure 5. Layout of the multiple-stage six-input NAND implementation.

| Implementation | No. of transistors | Area ($\mu$m) |
|---|---|---|
| One-stage NAND-6 | 12 | 48·6 × 32·6 |
| Multiple-stage NAND-6 | 20 | 102·2 × 32·6 |

Table 5. Number of transistors and area of the two implementations.

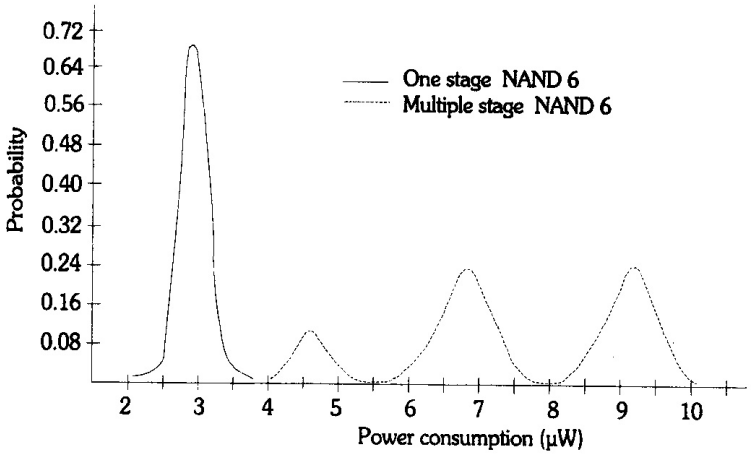


Figure 6. Power consumption histograms.

distribution of the power-delay product of both implementations (see Fig. 7). In this way, the mean power-delay product is computed similarly by

$$\overline{P \times D} \pm t_{a/2} \frac{s}{\sqrt{N}} \tag{15}$$

where $\overline{P \times D}$ is the sample average. However, since elongated tails occur at the power-delay curve of the multiple-stage implementation, a higher confidence

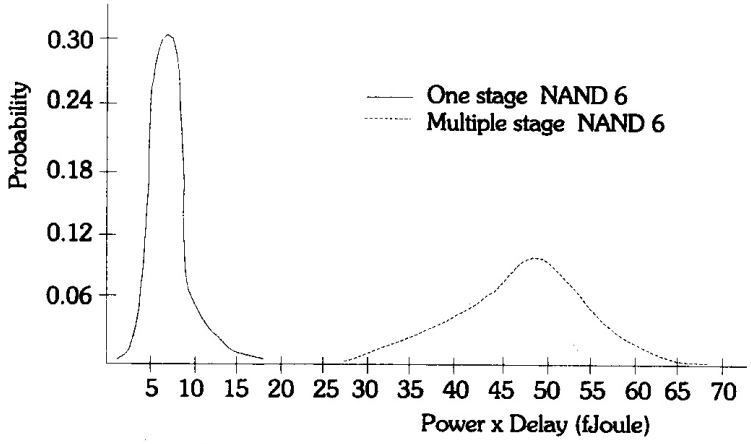


Figure 7. Power-delay product histograms.

| Samples ($N$) | $t_{a/2}$ | Confidence |
|---|---|---|
| 63 | 2 | 95% |
| | 2·6 | 99% |

Table 6. Percentile values $t_{a/2}$ for the $t$-distribution.

interval must be chosen to achieve better accuracy. Thus, the confidence of the one-stage implementation power and power-delay probability distributions is set to 95%, and the confidence of the multiple-stage implementation power–delay distribution to 99%. In Table 6 the values of the coefficient $t_{a/2}$ for $N=63$ and confidence 95% and 99% are given (Miller *et al.* 1990).

It can be observed in Fig. 6 that the probability distribution of the power consumption for the multiple-stage implementation is multimodal (with many humps); thus it cannot be approximated to normal (Burch *et al.* 1993, Schmitt 1969). However, this distribution can be approximated to three individual normal distributions, in which the statistical mean is given by (14), and we will refer to the overall distribution as a triple normal. The left part of this triple normal distribution contains nine samples, and the other two parts contain 27 samples each. By combining this with the power-consuming transition probabilities at the nodes of the multiple-stage implementation presented in the §2.2, the following results are extracted.

The nine input change samples of the left normal distribution result in a power-consuming transition (low to high) at one of the first stage nodes (outputs of the two-input NAND gates) and at the primary output node (see Fig. 3). The 27 samples of the middle normal distribution result in a power-consuming transition at two of the first stage nodes and at the primary output node. Finally, the 27 samples of the right normal distribution result in a power-consuming transition at all the first stage nodes and at the primary output node. Table 7 shows the conditional probabilities (Miller *et al.* 1990) of the events which are described in the above results.

Furthermore, it is considered that there are three operation modes, related to the power consumption in the multiple-stage implementation, when a power-consuming transition at the primary output node occurs. These modes of operation are considered as follows: when E1 and E4 events (Table 7) occur simultaneously as the mode A operation, when E2 and E4 events occur simultaneously as the mode B

| | |
|---|---|
| Events | E1 = 0→1 transition at the output of only one 2-input NAND gate |
| | E2 = 0→1 transition at the outputs of two 2-input NAND gates |
| | E3 = 0→1 transition at the outputs of all 2-input NAND gates |
| | E4 = 0→1 transition at the primary output node |
| Conditional probabilities | $P(E1/E4)=9/63$ |
| | $P(E2/E4)=27/63$ |
| | $P(E3/E4)=27/63$ |

Table 7. Conditional probabilities for the multiple-stage implementation.

| Six-input NAND gate | | Mean power dissipation per input change ($\mu$W) | Mean power × delay per input change (fJ) |
|---|---|---|---|
| One-stage implementation | | $2{\cdot}867 \pm 0{\cdot}0553$ | $6{\cdot}471 \pm 0{\cdot}8972$ |
| Multiple-stage implementation | mode A | $4{\cdot}529 \pm 0{\cdot}1228$ | $48{\cdot}960 \pm 3{\cdot}0749$ |
| | mode B | $6{\cdot}921 \pm 0{\cdot}0886$ | |
| | mode C | $9{\cdot}351 \pm 0{\cdot}1078$ | |

Table 8. Power and power-delay product measures for both implementations.

operation, and when E3 and E4 events occur simultaneously as the mode C operation.

By using the parameters of the probability distributions shown in Figs 6 and 7, (14), (15) and the data of Tables 6 and 7, the final results for the power and power-delay product of both implementations are computed. These results are given in Table 8. Note that for the computation of the mean power dissipation, for the three operation modes of the multiple-stage implementation, a confidence of 95% is used.

From Table 8 one can conclude that the power and the power-delay characteristics of the one-stage implementation are much better than those of the multiple-stage implementation. This is mainly due to the large internal switched capacitance of the multiple-stage implementation. An important issue is that the mean power dissipation of the multiple-stage implementation is higher than that of the one-stage implementation for all the operation modes (A, B, C). This is due to the fact that in the first implementation at least one more power-consuming transition occurs. The same result can be expressed from the probability distribution histograms (Fig. 6), since the curve of the multiple-stage implementation is on the right side of the one-stage implementation curve, in both power and power-delay product histograms.

Thus, it is found that for low-power digital design the one-stage implementation of a multi-input gate is better than its decomposition into simple gates. This is valid for multi-input gates with a number of inputs different than six, due to the fact that in any case the multiple-stage implementations present more power-consuming transitions per input change than the one-stage implementations.

## 4. Conclusions

In this paper the power and the power-delay product of two implementations for multi-input gates were compared. It has been shown that the power and power-delay characteristics of the one-stage implementation are better than those of the implementation where the multi-input gates are decomposed into simple gates. This has been proven by two approaches. In the first one probabilistic methods in estimating the average power dissipation (dynamic and short-circuit) were used, and in the second one a statistical approach that combines the speed of the probabilistic methods and the accuracy of the simulation-based methods was followed.

## References

BURCH, R., NAJM, F., YANG, P., and TRICK, T., 1993, A Monte Carlo approach for power estimation. *IEEE Transactions on VLSI Systems*, **1**, 63–71.

CHANDRAKASAN, A., SHENG, S., and BRODERSEN, R., 1992, Low-power CMOS digital design. *IEEE Journal of Solid-state Circuits*, **27**, 473–484.

CHANDRAKASAN, A., ALLMON, R., STRATAKOS, A., and BRODERSEN, R., 1994, Design of portable systems. *Proceedings of IEEE Custom Integrated Circuits Conference*, pp. 259–266.

DEVADAS, S., KEUTZER, K., and WHITE, J., 1992, Estimation of power dissipation in CMOS combinational circuits using boolean function manipulation. *IEEE Transactions on Computer-aided Design*, **11**, 373–383.

KANG, S., 1986, Accurate simulation of power dissipation in VLSI circuits. *IEEE Journal of Solid-state Circuits*, **21**, 889–891.

LIU, D, and SVENSSON, C., 1993, Trading speed for low power by choice of supply and threshold voltages. *IEEE Journal of Solid-state Circuits*, **28**, 10–17; 1994, Power consumption estimation in CMOS VLSI chips. *IEEE Journal of Solid-state Circuits*, **29**, 663–670.

META-SOFTWARE, 1992, *HSPICE User's Manual Version H92* (Campbell, Calif.: Meta-Software).

MILLER, I. R., FREUND, J. E., and JOHNSON, R., 1990, *Probability and Statistics for Engineers (Englewood Cliffs, NJ: Prentice Hall)*.

NAJM, F., 1993, Transition density: a new measure of activity in digital circuits. *IEEE Transactions on Computer-aided Design*, **12**, 310–323; 1994, A Survey of power estimation techniques in VLSI circuits. *IEEE Transactions on VLSI Systems*, **2**, 446–455.

ROUATBI, F., HAROUN, B., and AL-KHALILI, A. J., 1992, Power estimation tool for sub-micron CMOS VLSI circuits. *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 204–209.

RUBENSTEIN, J., PENFIELD, P., and HOROWITZ, M. A., 1983, Signal delay in RC networks. *IEEE Transactions on Computer-Aided Design*, **2**, 202–211.

SCHMITT, S. A., 1969, *Measuring Uncertainty: an Elementary Introduction to Bayesian Statistics* (Massachusetts: Addison-Wesley).

SHIMOHIGASHI, K., and SEKI, K., 1993, Low-voltage ULSI design. *IEEE Journal of Solid-state Circuits*, **28**, 408–413.

VEENDRICK, H. J. M., 1984, Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits. *IEEE Journal of Solid-state Circuits*, **19**, 468–473.

VITTOZ, E., 1994, Low-power design: ways to approach the limits. *Proceedings of the Institute of Electrical and Electronics Engineers. International Solid-state Circuits Conference*, pp. 14–18.

WESTE, N, and ESHRAGIAN, K., 1992, *Principles of CMOS VLSI Design: a Systems Perspective* (Massachusetts: Addison-Wesley).