An Accurate and Compact MOSFET I-V Model for Nanometer CMOS Circuit Analysis

Labros Bisdounis

Electrical Engineering Department
Technological Educational Institute of Patras
GR-26334 Patras, Greece

***Abstract*—The analysis and modeling of digital CMOS circuits' dynamic characteristics (such as propagation delay, transition time, energy dissipation), require a MOSFET I-V model that combines accuracy, by including the influences of the main modern technologies effects, and simplicity, in order to provide the ability for closed-form expressions derivation. It is obvious that the accuracy of the I-V model for nanometer devices determines to a large extent the accuracy of CMOS circuits' timing and energy characteristics modeling. In this paper, an accurate and compact MOSFET I-V model that takes into account the influences of predominant effects in nanometer device technologies is presented. The model has been validated for several sub-100nm CMOS technologies and for different device widths. The experimental results show very good agreement with BSIM4 HSPICE simulations.**

***Keywords*—Nanometer MOSFETs, Semiconductor device modeling, CMOS circuit analysis.**

I. Introduction

Estimation of digital circuits' behavior, in terms of analysis and computation of their dynamic characteristics, is today a standard part of integrated circuit design. The usefulness and the efficiency of such processes depend on the adequacy of the used device models [1]–[2]. In particular, the accuracy and simplicity (computational efficiency) of the used MOSFET model directly affects the accuracy and speed of circuit analysis.

Most of the MOSFET models that are currently used for circuit analysis and simulation are semi-empirical analytical models, in which the effects that determine the device behavior are accounted for through physical and empirical parameters [3]–[9].

Generally, the models, in order to be acceptable and useful to the designers, must meet application specific requirements. In digital CMOS design, accurate drain current prediction (i.e. accurate I-V equations) is a key requirement. In addition, when the purpose is to analyze CMOS circuits by obtaining explicit closed-form expressions for design parameters, such as delay and energy dissipation [10]–[12], the simplicity of the device model equations is an equally important requirement. With the growing complexity of physical mechanisms in deep-submicrometer and nanometer devices, semi-empirical analytical MOSFET models become very complex and employ a large number of parameters to provide the highest accuracy [3]–[4]. Although these complex but accurate models can be handled by circuit simulators [13], they do not satisfy the requirement of computational efficiency.

This is the main reason for compact MOSFET models development, in which the I-V equations should be as simple as possible to take into account the influences of essential physical mechanisms in nanometer devices by using few parameters extracted through measurements or simulations [3], [14]–[21]. These I-V equations use empirical parameters to specifically match measured device characteristics. Some of these parameters typically do not have a physical relation with the underlying device mechanism, and they are referred as fitting parameters, since they fit a measured curve with a mathematical expression.

In this paper, an accurate and compact I-V model for nanometer MOSFETs is proposed. Existing compact short-channel MOSFET models (namely the alpha-power and nth-power law models [16]–[17]) are used as a basis, to develop an I-V MOSFET model that takes into account the influences of predominant effects in nanometer device technologies, such as: carriers' velocity saturation, mobility degradation, body effect, channel-length modulation, drain-induced barrier lowering (DIBL), source-drain parasitic resistance, narrow channel width effects. The derived MOSFET model describes accurately the strong inversion device current, providing the ability for accurate and analytical computation of CMOS circuits' design parameters such as delay, transition time, and energy dissipation.

II. MOSFET I-V Model

The basic concept of the compact short-channel MOSFET models published in [16]–[17] is that the transistor drain current is proportional to $(V_{GS}-V_{TH})^{\alpha}$, where V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage and alpha is the velocity saturation index. Before the suggestion of this model, several models were proposed, but they were far more complicated, and manipulating the models analytically did not give fruitful results for circuit designers. When the model was first introduced, it was purely empirical, without physical background. However, afterwards the physical interpretation of the alpha-power dependency was investigated by multiple authors [19], [22]–[23] and it was determined that the origin of such dependency is based on mobility degradation at high electric fields. In addition, relations between the model's empirical parameters and physical parameters were provided. In the initial version of the model [16], carriers' velocity saturation and mobility degradation effects were modeled in a very compact way. The model was revisited in [17], in order to include the influences of channel-length modulation and body biasing [24]. However, the influence of second-order effects that are predominant in nanometer MOSFETs, was not modeled.

The device I-V model, described below, is an attempt to include the influences of additional effects [24] such as drain-induced barrier lowering (DIBL), source-drain parasitic resistance, and narrow channel width effects in a very compact way. The device drain current is expressed as:
For $V_{DS} \le V'_{DO}$ (triode region),

$$I_D = B_{tri}\,(V_{GS} - V_{TH})^{\alpha}\left(2 - \frac{V_{DS}}{V'_{DO}}\right)\frac{V_{DS}}{V'_{DO}}, \qquad (1)$$

For $V_{DS} > V'_{DO}$ (saturation region),

$$I_D = B_{sat}\,(V_{GS} - V_{TH})^{\alpha}\left[A + D\,(V_{DS} - V_{DO})\right], \qquad (2)$$

where

$$V'_{DO} = V_{DO}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\frac{a}{2}}, \qquad (3)$$

$$V_{TH} = V_{TO} + \gamma V_{SB}, \qquad (4)$$

$$B_{tri} = \frac{I'_{DO}}{(V_{DD} - V_{TH})^{\alpha}},\ B_{sat} = \frac{I_{DO}}{(V_{DD} - V_{TH})^{\alpha}},\ A = \frac{I'_{DO}}{I_{DO}},$$

$$\text{and } D = \frac{1 - A}{V_{DD} - V_{DO}}.$$

V_{GS}, V_{DS}, V_{SB}, V_{DD}, and V_{TH} are gate-source, drain-source, source-bulk, supply, and threshold voltage, respectively. α is the velocity saturation index, V_{TO} stands for the zero back-gate bias threshold voltage, and γ is a coefficient accounts for the body effect. V'_{DO} is the drain-source saturation voltage, and V_{DO} is the drain-source saturation voltage at $V_{GS} = V_{DD}$. B_{tri} and B_{sat} are transconductance parameters for triode and saturation region, respectively. I_{DO} is the drain current at $V_{GS} = V_{DS} = V_{DD}$, while I'_{DO} is the drain current at $V_{GS} = V_{DD}$, and $V_{DS} = 1/2\,V_{DD}$ (for the NMOS device), $V_{DS} = 2/3\,V_{DD}$ (for the PMOS device).

The first step to extract the model parameters is the selection of fitting points on the device I-V curves. The proper fitting points to predict the drain current of the NMOS device are indicated in Fig. 1. The fitting points for the PMOS device are selected similarly according to the aforementioned details. I_{DO}, I'_{DO} are easily obtained from the output MOSFET characteristics (points 5 and 4, respectively). α is extracted from the following equation which is derived from (2) by using the fitting points 2 and 3 [16]:

$$\alpha = \frac{\ln\left(\frac{I_{D3}}{I_{D2}}\right)}{\ln\left(\frac{V_{GS3} - V_{TO}}{V_{GS2} - V_{TO}}\right)} \qquad (5)$$

V_{DO} is computed by combining (1) and (3) and using $V_{GS} = V_{DD}$, $V_{DS} = 1/4\,V_{DD}$, (fitting point 1) as well as the corresponding drain current value (I_{D1}):

$$V_{DO} = \frac{I'_{DO}\,V_{DD} + V_{DD}\sqrt{I'_{DO}(I'_{DO} - I_{D1})}}{4\,I_{D1}}. \qquad (6)$$

For a given nanometer technology, the values of the model parameters are derived for the minimum device width. In order to extend the model for higher device channel widths (W), the values of the transconductance parameters (B_{tri}, B_{sat}) and consequently the values of the parameters I_{DO}, I'_{DO} are extracted by using the following equations:

$$B_{tri} = \beta_{t1} + \beta_{t2} W + \beta_{t3} W^2 \qquad (7a)$$

$$B_{sat} = \beta_{s1} + \beta_{s2} W + \beta_{s3} W^2 \qquad (7b)$$

where the coefficients β_{ti} and β_{si} are determined by fitting quadratic plots to the B_{tri} vs W and B_{sat} vs W plots, respectively (once for a given nanometer technology) [25].

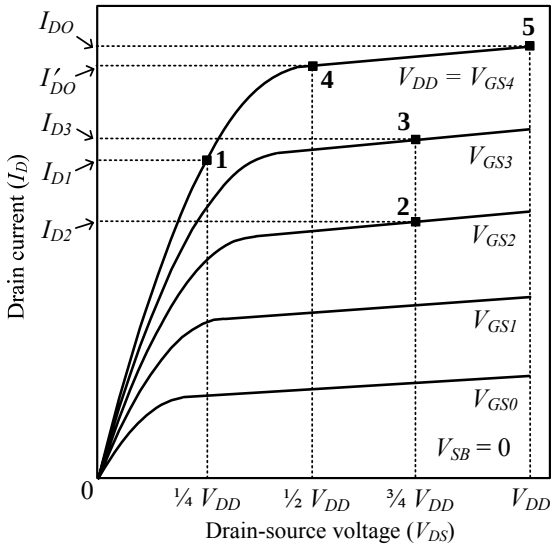

Figure 1. Selected points for NMOS parameters extraction

For the determination of the device threshold voltage for the cases where $V_{SB} \neq 0$, a linear approximation (4) of the BSIM4 expression describing the body effect [4] is used. The BSIM4 expression is:

$$V_{TH} = V_{TO} + K_1\left(\sqrt{\varphi_s + V_{SB}} - \sqrt{\varphi_s}\right) + K_2 V_{SB}, \qquad (8)$$

where φ_s is the strong inversion surface potential, and K_1, K_2 are the BSIM4 body effect coefficients. To extract the value of coefficient γ, an adjustment of the linear expression (4) to (8) is performed at $V_{SBf} = 1/3\,V_{DD}$:

$$\gamma = \frac{V_{THf} - V_{TO}}{V_{SBf}} \qquad (9)$$

where $V_{THf} = V_{TO} + K_1\left(\sqrt{\varphi_s + V_{SBf}} - \sqrt{\varphi_s}\right) + K_2 V_{SBf}$.

The modeling of velocity saturation and mobility degradation effects is achieved by employing the velocity saturation index (α) to describe the power laws featuring the drain current and the drain-source saturation voltage. The dependence between the drain current and the drain-source voltage in the saturation region, which is mainly due to the channel-length modulation and drain-induced barrier lowering (DIBL) effects, is modeled through the inclusion of parameters A and D to the presented I-V model. The prediction of the drain current for varying device widths (i.e. the inclusion of narrow channel width effects [1]) is obtained by computing the transconductance parameters in both triode and saturation regions as quadratic functions of the channel width. Finally, the source-drain parasitic resistance effect, which causes drain current degradation mainly in the triode region [3],[24], is taken into account by using lower transconductance parameter in the triode region than that in the saturation region.

III. Experimental Results and Conclusion

The derived MOSFET model has been initially validated by using a 90nm CMOS technology. Fig. 2 presents the NMOS and PMOS I-V curves for device widths 120 nm and 280nm, respectively. The values of the presented model parameters are listed in Table I. The results show very good agreement with BSIM4 HSPICE simulations. The device model parameters used to obtain the presented BSIM4 [4] HSPICE [13] simulation results have been extracted by the online available tool [26] in the Predictive Technology Model [27] website. In Fig. 3, the presented model is validated for several device widths, and the results are similarly accurate.

Finally, in Fig. 4, the results extracted by the presented MOSFET I-V model are provided, along with the corresponding BSIM4 HSPICE simulations, for two additional sub-100nm CMOS technologies (65nm, 45nm). Note, that in Figs. 2, 3, and 4 continuous lines correspond to the model results, while dots correspond to the BSIM4 HSPICE simulations.

The discontinuity at the boundary between triode and saturation regions, does not affect significantly the accuracy of the presented model, in which complex dependences on drain-source voltage are avoided. Such discontinuity could cause problems in computer simulators, which require continuity of the functions as well as of the derivatives, but should not cause problems in case of use for analytical computation of design parameters.

As a conclusion, the presented MOSFET I-V model combines accuracy (since it accounts for the influences of the essential effects in modern CMOS technologies), and simplicity to provide the ability for explicit expressions derivation for design parameters, such as delay, transition time and energy dissipation. The accuracy of the model has been validated for several sub-100nm CMOS technologies, device widths, and supply voltages.

TABLE I. Model Parameter values for 90nm CMOS Technology

Model parameters	W [nm]	α [ ]	I_{DO} [μA]	I'_{DO} [μA]	V_{DO} [V]	V_{TO} [V]	γ [ ]	φ_s [V]	K_1 [$V^{1/2}$]	K_2 [ ]
NMOS device	120	1.072	118.78	110.55	0.579	0.290	0.196	0.873	0.383	0.01
PMOS device	280	1.298	119.10	109.86	–0.847	–0.236	0.201	0.865	0.340	–0.01

Transconductance coefficients	b_{t1} [A/V^{α}]	b_{t2} [$A/m \cdot V^{\alpha}$]	b_{t3} [$A/m^2 \cdot V^{\alpha}$]	b_{s1} [A/V^{α}]	b_{s2} [$A/m \cdot V^{\alpha}$]	b_{s3} [$A/m^2 \cdot V^{\alpha}$]
NMOS device	-13.393×10^{-6}	1131.84	-8.2901×10^{6}	-8.420×10^{-6}	1165.49	-3.4340×10^{5}
PMOS device	-22.373×10^{-6}	1177.54	-2.5811×10^{8}	-24.280×10^{-6}	1276.82	-2.8003×10^{8}

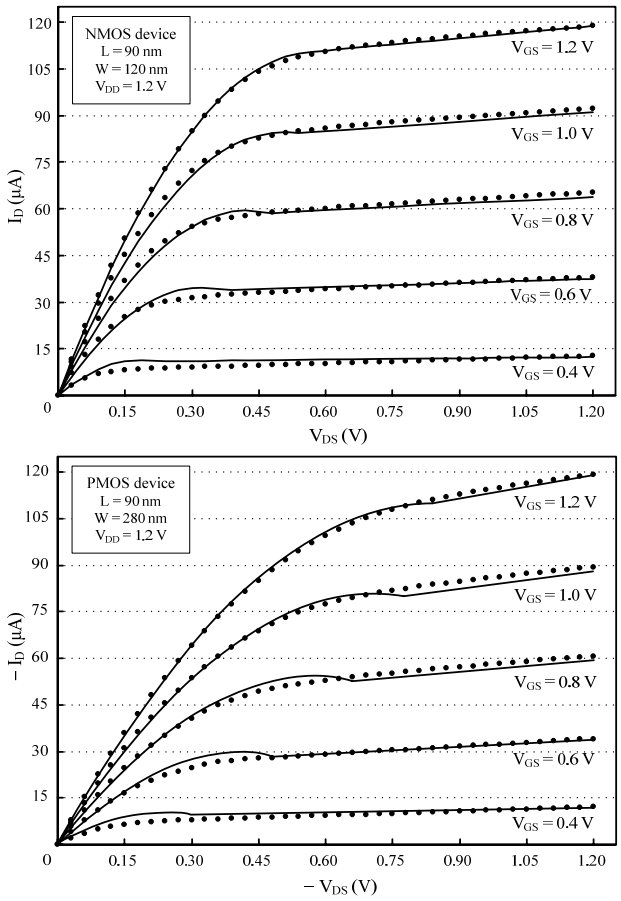

Figure 2. I-V plots for 90nm CMOS technology

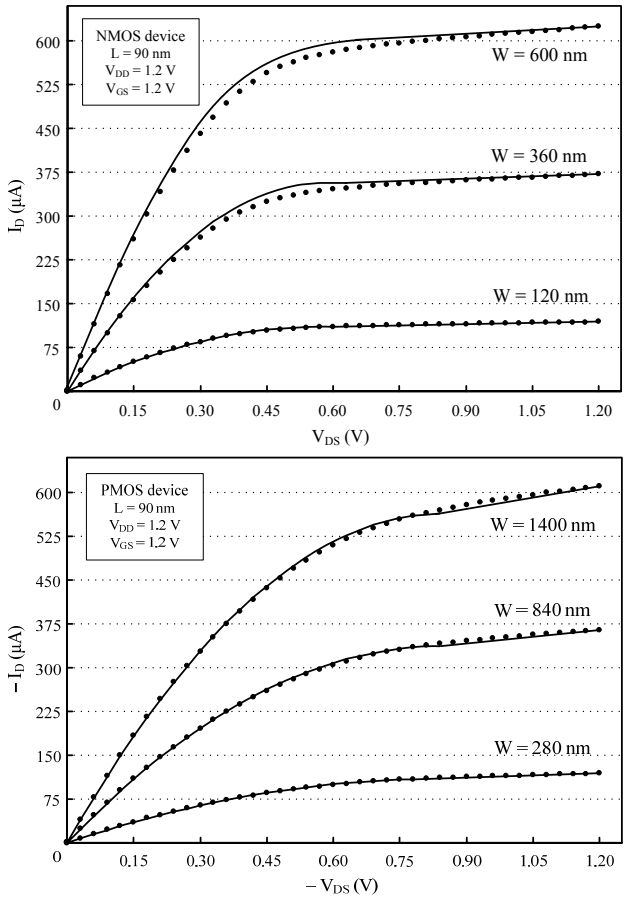

Figure 3. I-V plots for different device channel widths

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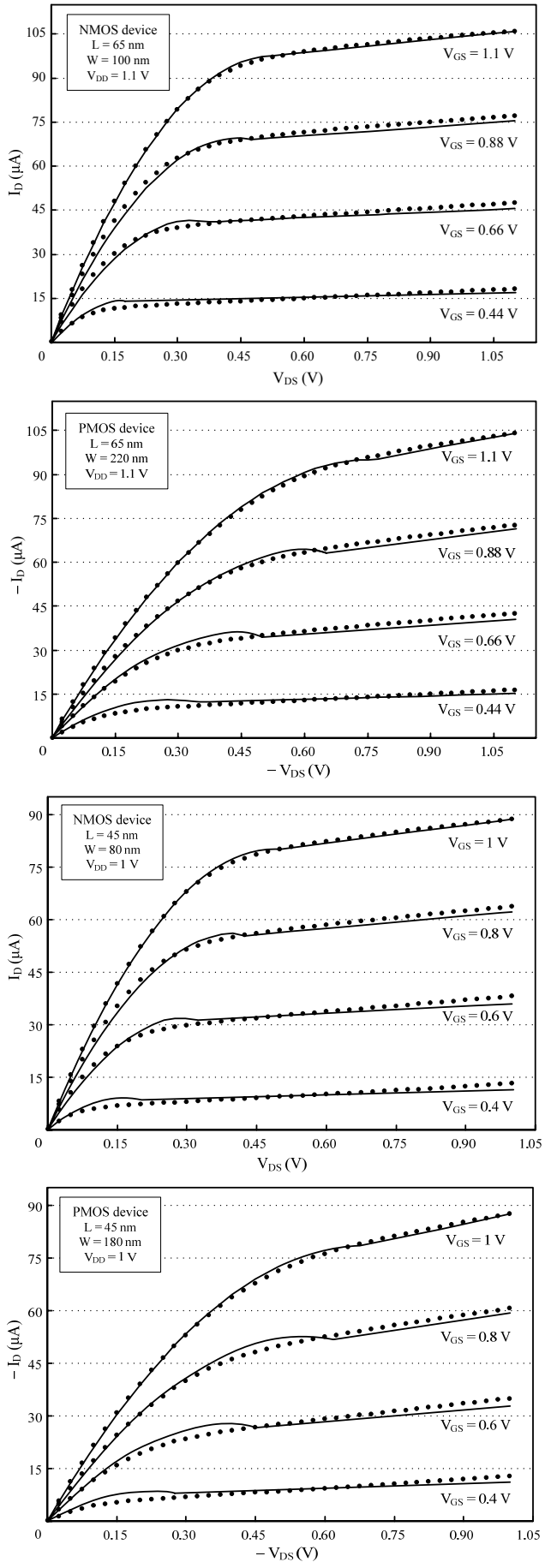

Figure 4. I-V plots for 65nm and 45nm CMOS technologies

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