SHORT-CIRCUIT ENERGY DISSIPATION MODEL FOR SUB-100nm CMOS BUFFERS

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ABSTRACT

A considerable part of the energy dissipation in CMOS buffers is due to short-circuit currents. In this paper, an accurate, analytical and compact model for this part of energy, i.e. the short-circuit energy dissipation, is presented. The model is based on closed-form expressions of the CMOS inverter output waveform, which include the influences of both transistor currents and the gate-drain coupling capacitance. An accurate version of the alpha-power law MOSFET model is used to relate the terminal voltages to the drain current in sub-100nm devices, with an extension for varying transistor widths. The resulting energy model accounts for the influences of input voltage transition time, transistors' sizes, device carrier velocity saturation and narrow-width effects, gate-drain and short-circuiting transistor's gate-source capacitances, and output load. The model has been validated for a 90-nm CMOS technology, for different input transition times, capacitive loads & inverter sizes. The results show very good agreement with BSIM4 HSPICE simulations.

Index Terms— CMOS buffers, circuit modeling, short-circuit power dissipation, nanometer MOSFETs.

1. INTRODUCTION

Energy dissipation is a very critical parameter that has to be taken into account during the design of VLSI circuits, to avoid problems related to heating in high-performance applications and to energy savings in battery-oriented portable applications. Thus, computer-aided design tools should include efficient methods for fast and accurate computation of energy dissipation. It is well-known that the dynamic part of energy dissipation in CMOS structures is caused by charging/discharging the output load and by the short-circuit current that flows from the power supply to the ground, during switching of structures [1]. The importance of modeling short-circuit energy dissipation of CMOS buffers, comes from the fact that a great fraction of the energy dissipated in VLSI circuits is due to the clock driving circuits and I-O drivers, which are based to inverting buffers [2]. In addition, an analytical model of the energy dissipated by an inverter can be used in conjunction with several reduction methods of CMOS gates to equivalent inverters [3].

Several models [4]-[13] have been proposed to compute the short-circuit energy dissipation of a CMOS inverter. In [4] an expression for the evaluation of the short-circuit energy dissipation with the assumption of zero load was proposed, that gives pessimistic results due to the strong dependence of the short-circuit energy on the load capacitance. In [5] an expression without the zero-load simplification was presented. However, it was based on the well-known square-law MOSFET model that ignores the carriers' velocity saturation effects of sub-micron and nanometer devices. In [6], an improved model was proposed that includes the influences of the short-circuit current and the gate-drain coupling capacitance on the inverter output waveform, while still based on the square-law device model. The expression presented in [7] is an extension of the zero-load model presented in [4], based on the alpha-power law MOSFET model, which is valid for short-channel devices. The work of Vemuru et al. [8], is based on the same device model, it covers loaded buffers, however, the used output waveform expression does not include the influences of the short-circuit current and the gate-drain coupling capacitance. In [9], the short-circuit current waveform was approximated with a piecewise linear function of time in all operating regions, in order to estimate the short-circuit charge and energy dissipation. Similar piecewise linear functions of the short-circuit current were used in the models presented in [10] and [11], in which approximations were used for the calculation of the required current waveform points, while in [10] numerical computing is required. Turgis et al. [12] derived a model in which the short-circuit energy dissipation is computed through a fictitious short-circuit capacitance. The inverter output is approximated by a linear waveform that uses empirical fitting parameters and the same short-circuiting transistor's charge is assumed in both linear and saturation regions. The expression proposed by Nose et al. [13], takes into account short-channel effects, while uses assumptions such as negligible short-circuit current and zero coupling capacitance during the derivation of the output signal expression. Both influences are included in the energy model derived in [3], however a linear expression for the devices' drain current in the triode operating region is used, and the reported error reaches 15% for submicron transistors.

In this paper, an accurate, analytical and compact model for the computation of the CMOS short-circuit energy dissipation, is presented. It is based on a version of the alpha-power law MOSFET model [13] that uses an accurate device drain current expression in the triode operating region, rather than the linear expression proposed in [7]. In addition, an extension [14] of the device model is used to cope with narrow-width effects of sub-100nm devices. For the derivation, analytical expressions of the output waveform in the operating regions, which are required for the evaluation of the short-

circuit energy dissipation, are used. These expressions take into account the current through both transistors and the influence of the gate-drain coupling capacitance, and they are valid for a wide range of input transition times, output loads, supply voltages and device sizes. In addition, the influence of the short-circuiting transistor's gate-source capacitance is included, when computing the short-circuit energy dissipation of the inverter.

2. MOSFET MODEL

For the expressions of the transistors' drain current, the following accurate and simple version of the alpha-power law MOSFET model is used [7],[13].

For $V_{DS} > V'_{DO}$ (saturation region):

$$I_D = B(V_{GS} - V_T)^{\alpha} \quad (1)$$

For $V_{DS} \le V'_{DO}$ (triode or linear region):

$$I_D = B(V_{GS} - V_T)^{\alpha}\left(2 - \frac{V_{DS}}{V'_{DO}}\right)\frac{V_{DS}}{V'_{DO}} \quad (2)$$

where $V'_{DO} = K(V_{GS} - V_T)^{\frac{\alpha}{2}}$, $K = V_{DO} / (V_{DD} - V_T)^{\frac{\alpha}{2}}$, (3)

V_{DD}: supply voltage, α: velocity saturation index (extracted as mentioned in [7]), V'_{DO}: drain-source saturation voltage, B: transconductance parameter, V_T: threshold voltage. The saturation voltage at $V_{GS} = V_{DD}$ (V_{DO}) is computed as follows, by combining equations (1)-(3) and using the coordinates (I_{DSA}, V_{DSA}) of an output MOSFET characteristics point (A), close to the middle of the linear region:

$$V_{DO} = \frac{BV_{DSA}(V_{DD} - V_T)^{\alpha} + \sqrt{BV_{DSA}^2(V_{DD} - V_T)^{\alpha}[B(V_{DD} - V_T)^{\alpha} - I_{DSA}]}}{I_{DSA}}.$$

B is calculated from eq. (1) by using the drain current extracted from the output MOSFET characteristics for $V_{GS} = V_{DD}$ and $V_{DSC} = 3/4 \cdot V_{DD}$ (for NMOS device), $V_{DSC} = 4/5 \cdot V_{DD}$ (for PMOS device), in order to compensate inaccuracies due to channel length modulation. The used MOSFET model is more accurate for sub-100nm devices than the classic alpha-power model that uses linear drain current at the triode region, as shown in Fig. 1, in which points A, C used for the extraction of parameters V_{DO} and B are also indicated. B is extracted for the minimum device width. To extend the model for higher device channel widths (W), the following equation is used [14]:

$$B = \beta_1 + \beta_2 W + \beta_3 W^2, \quad (4)$$

where the coefficients β_i are determined by fitting a quadratic plot to the B vs W plot (once for a given technology).

3. SHORT-CIRCUIT ENERGY DISSIPATION

The derivations presented in the following are for a rising input ramp: $V_{in} = V_{DD} \cdot (t / \tau)$ for $0 \le t \le \tau$, $V_{in} = 0$ for $t \le 0$ and $V_{in} = V_{DD}$ for $t \ge \tau$, where τ is the input rise time. The analysis for a falling input is symmetrical. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter (Fig.2), taking into account the current through the gate-drain coupling capacitance (C_M) is written as

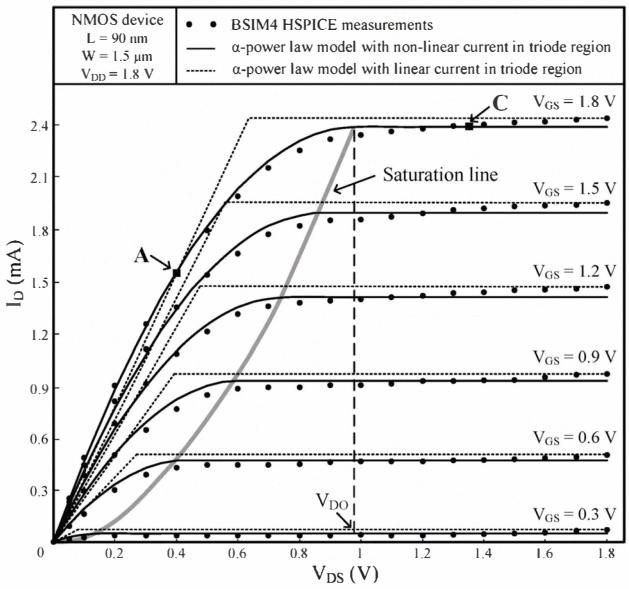

Fig. 1: 90-nm NMOS device I-V plots

$$C_L \frac{dV_{out}}{dt} = C_M\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) + I_p - I_n. \quad (5)$$

The gate-drain capacitance (C_M) is the sum of the gate-drain capacitances of both transistors, which consist of the gate-to-drain overlap capacitance and a part of the gate-to-channel capacitance. It is calculated by using C_{ox} (gate-oxide capacitance per unit area) and C_{gdo} (gate-drain overlap capacitance per unit channel width) [1].

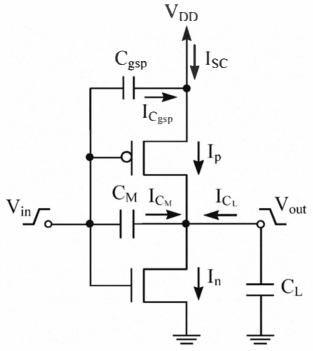

Fig.2: The CMOS inverter

After normalizing voltages with respect to V_{DD}, i.e. $u_{in} = V_{in} / V_{DD}$, $u_{out} = V_{out} / V_{DD}$, $n = V_{TN} / V_{DD}$, $p = |V_{TP}| / V_{DD}$, $u'_{don} = V'_{DON} / V_{DD}$, $u'_{dop} = V'_{DOP} / V_{DD}$ and using the variable $x = t / \tau$, the PMOS device current is given by

$$I_p = \begin{cases} k_{lp1}(1 - x - p)^{\alpha_p/2}(1 - u_{out}) - k_{lp2}(1 - u_{out})^2, & 1 - u_{out} < u'_{dop} \quad (6a) \\ k_{sp}(1 - x - p)^{\alpha_p}, & 1 - u_{out} \ge u'_{dop} \quad (6b) \end{cases}$$

where $k_{lp1} = \frac{2B_P V_{DD}^{(\alpha_p+2)/2}}{K_P}$, $k_{lp2} = \frac{B_P V_{DD}^2}{K_P^2}$, $k_{sp} = B_P V_{DD}^{\alpha_p}$,

$$u'_{dop} = k_{vp}(1 - x - p)^{\alpha_p/2}, \; k_{vp} = K_P V_{DD}^{(\alpha_p - 2)/2}.$$

The NMOS device current is given in a similar way. For the evaluation of the short-circuit energy dissipation, analytical expressions of the output waveforms in the two first inverter operation regions (Fig. 3) are required.

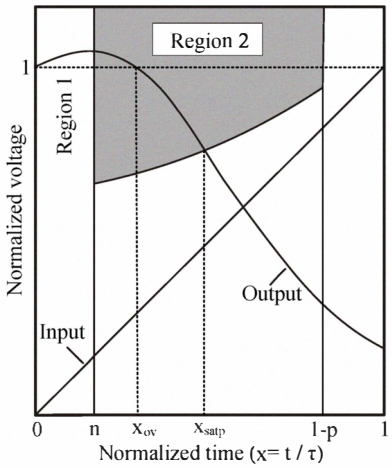

Fig. 3: Inverter operating regions

In region 1 ($0 \le x \le n$) the NMOS transistor is off and the PMOS transistor is in the linear region, while in region 2 ($n \le x \le x_{satp}$) the NMOS transistor is saturated and the PMOS transistor is still in the linear region. x_{satp} is the normalized time value when the PMOS transistor is entering the saturation region. Part of the charge from the input which injected through the gate-drain coupling capacitance causes an overshoot at the beginning of the output signal transition ($0 \le x \le x_{ov}$). During the overshoot there is no current from power supply to ground because the output voltage is greater than the supply voltage. A small amount of charge stored in the output node returns back to the supply node, slightly reducing the capacitive energy dissipation.

In region 1 ($0 \le x \le n$), the charge injected through C_M causes the main influence on the output signal. Since, (5) cannot be solved analytically, an average value of x ($x_{av} = n / 2$) is used in the first term of PMOS current, as well as an approximated expression for u_{out} ($u_{apr} = 1 + c_m x$, that is the output signal if only the charge through C_M is taken into account) in the quadratic term of the PMOS current. After that, u_{out} is given as

$$u_{out} = 1 + \frac{c_m}{C^3 A_{lp1}^3}\Big[2A_{lp2}c_m(e^{-xCA_{lp1}} - 1) + 2CA_{lp1}A_{lp2}c_m x + C^2 A_{lp1}^2(1 - e^{-xCA_{lp1}} - A_{lp2}c_m x^2)\Big] \quad (7)$$

where $c_m = \frac{C_M}{C_L + C_M}$, $C = \left(1 - p - \frac{n}{2}\right)^{\frac{\alpha_p}{2}}$, $A_{lpi} = \frac{\tau k_{lpi}}{V_{DD}(C_L + C_M)}$.

In region 2, the NMOS device is saturated, while the PMOS remains in the linear region. The PMOS current is approximated by a linear function of x (Fig.3):

$$I_p = I_{p(n)} + S_1(x - n).$$

$I_{p(n)}$ is calculated using the PMOS current expression in the linear region (eq. (6a)) and the value of the normalized output voltage at x = n (u_n, calculated by eq. (7)).

$$I_{p(n)} = k_{lp1}(1 - n - p)^{\alpha_p/2}(1 - u_n)$$

The current slope S_1 is computed by equating the PMOS current in the linear region (eq. (6a)) with the approximated one, at $x = (1 - p)/2$. The output voltage waveform is described by

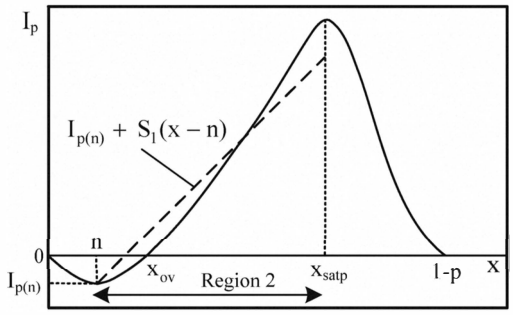

Fig. 4: PMOS current approximation in region 2

$$u_{out} = u_n + c_m(x - n) + I_{p(n)}d(x - n) + \frac{S_1 d(x - n)^2}{2} - \frac{A_{sn}(x - n)^{\alpha_n + 1}}{\alpha_n + 1} \quad (8)$$

where $d = \frac{\tau}{V_{DD}(C_L + C_M)}$ and $A_{sn} = \frac{k_{sn}\tau}{V_{DD}(C_L + C_M)}$.

The normalized time value x_{satp} satisfies the PMOS saturation condition: $u_{out} = 1 - u'_{dop}$. In order to solve this equation a Taylor series expansion around the point $x = 1 - p - n$ up to the second order coefficient is used, for both u_{out} and u'_{dop}. The normalized time value x_{ov} (end of the output signal overshoot) is calculated by the equation $u_{out} = 1$, using the Taylor series expansion of u_{out} around the point $x = 1.5 \cdot n$.

The short-circuit energy dissipation for a rising input is the energy of the current (I_{SC}) which provided from the power supply (Fig.2). The current through the PMOS device includes two non-short-circuit current components: the current flowing through C_{gsp} and the current flowing from the output to the supply node during the overshoot of the output signal. Both current components are provided from the input and are independent of the load. The short-circuit energy dissipation during a falling output transition is defined as

$$E_{SC} = V_{DD}\int_{x_{start}}^{x_{end}} I_{SC}\tau dx = V_{DD}\left(\int_{x_{start}}^{x_{satp}} I_{SC}\tau\, dx + \int_{x_{satp}}^{x_{end}} I_{SC}\tau\, dx\right) \quad (9)$$

where $I_{SC} = I_p - I_{C_{gsp}}$ and $I_{C_{gsp}} = C_{gsp}(V_{DD}/\tau)$.

In the first integral of (9) a linear approximation of the PMOS transistor current is used (Fig.5)

$$I_p = S_2(x - x_{ov}). \quad (10)$$

S_2 is the slope of I_p and is calculated by equating the PMOS current in the linear region (eq. (6a)) with that of (10), at the middle of the interval [x_{ov}, x_{satp}].

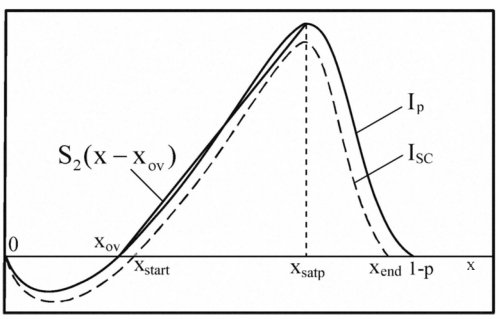

Fig. 5: Short-circuit current waveform

In the second integral of (9), the PMOS saturation current expression (eq. (6b)) is used. After that, the short-circuit energy dissipation expression becomes

$$E_{SC} = \frac{V_{DD}}{2}(x_{satp} - x_{start})[(x_{satp} + x_{start} - 2x_{ov})S_2 - \frac{2C_{gsp}V_{DD}}{\tau}] + \frac{V_{DD}k_{sp}\tau}{\alpha_p + 1}[(1 - p - x_{satp})^{\alpha_p+1} - (1 - p - x_{end})^{\alpha_p+1}] - C_{gsp}V_{DD}^2(x_{end} - x_{satp})$$

x_{start} is calculated by the equation

$$S_2(x_{start} - x_{ov}) - C_{gsp}(V_{DD}/\tau) = 0 \cdot$$

x_{end} is calculated by the equation

$$k_{sp}(1 - x - p)^{\alpha_p} - C_{gsp}(V_{DD}/\tau) = 0,$$

in which a second order Taylor series expansion of the first term around the point $x = [x_{satp} + 3(1 - p)]/4$, is used. The analysis of the short-circuit energy dissipation during the rising output transition is symmetrical.

4. RESULTS AND CONCLUSION

The model is validated for a 90-nm CMOS technology [15]. In Figures 6(a), 6(b), the short-circuit energy per transition is plotted for different input transition times, capacitive loads and inverter sizes. The results show very good agreement with BSIM4 HSPICE simulations (average error is about 3.5%). In addition, in Fig. 6(c), the short-circuit energy per transition is plotted as a function of the supply voltage, validating the accuracy of the model for the range of supply voltages applied in modern CMOS circuits. As a conclusion, the presented energy model accounts for the influences of input voltage transition time, transistors' sizes, device carrier velocity saturation and narrow-width effects, gate-drain and short-circuiting transistor's gate-source capacitances, output load and provides an analytical and accurate method for the evaluation of the short-circuit energy dissipation in sub-100nm CMOS buffers.

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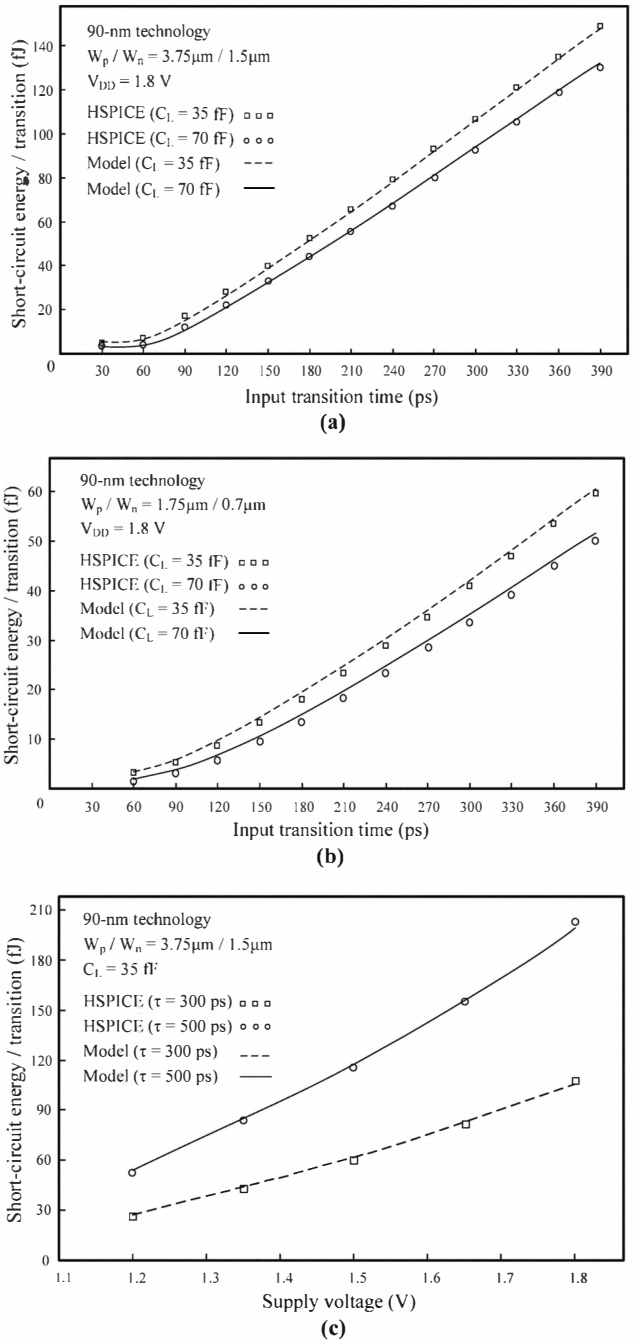

Fig.6: Short-circuit energy dissipation comparisons between presented model and SPICE simulations

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