TUD, POLITO, UP, IMEC, CSEM, LIRMM, OFFIS
present:

The SECOND

WORKSHOP

POLITECNICO DI TORINO

TORINO, ITALY

September 9, 2003

For Information and Registration:

http://www.lowpower.org

http://eda.polito.it/marlow

MARLOW: A central MARket-place for dissemination of LOW-power microelectronics design knowledge

Organizers:

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WORKSHOP PROGRAM

08.00-09.00:	Registration
09.00-09.15:	Welcome Enrico Macii, Politecnico di Torino, I
	The MARLOW Thematic Network Rene van Leuken, Delft Technical University, NL
09.15-10.00:	Keynote Speech 1 De-synchronization: How to transform a good synchronous circuit into a better asynchronous one. Prof. Jordi Cortadella, Universitat Politecnica de Catalunya, E
10.00-10.45:	Keynote Speech 2 Software Power Optimization: When, Where and How Prof. Luca Benini, Universita` di Bologna, I
10.45-11.15:	Coffee Break
11.15-12.30:	The MARLOW Low-Power Roadmap Dr. Johan Vounkx, IMEC, B
	Open discussion
12.30-14.15:	Lunch
14.15-15.30:	Short Course (part I) Low Power Issues in VLSI Testing Prof. Dimitris Nikolos, University of Patras, GR
15.30-15.45:	Coffee Break
15.45-17.00:	Short Course (part II) Low Power Issues in VLSI Testing Prof. Dimitris Nikolos, University of Patras, GR
17.00-18.00:	Special Session (invited presentations)
	Energy-Aware System-on-Chip (SoC) Design for 5 GHz WLANs Dr. Labros Bisdounis, INTRACOM S.A., GR
	Instruction-Level Energy Characterization of an ARM Processor Prof. Spiros Nikolaidis, AUTH, GR
	Energy-Efficient Memory and Bus Interface Design of the EASY Chip Dr. Elvira Omerbegovic, BullDAST s.r.l., I
18.00:	Closing

Energy-aware system-on-chip (SoC) design for 5 GHz WLANs

Dr. Labros Bisdounis

INTRACOM S.A., Greece

Abstract

The main technical objective of the IST project EASY is to develop a low power System-on-Chip (SoC) capable to undertake the baseband, MAC and DLC processing of a 5 GHz wireless system (based on theHIPERLAN/2 standard, but also implementing critical processing of the IEEE 802.11a standard).

The design flow starts with the definition of the system's parameters and requirements, the development of a high-level system model and the definition of the architectural template. The procedure is continued with a power-conscious mapping of the system's functionality, the real-time embedded software development, the hardware design and integration, the FP GA prototyping, the SoC fabrication and testing, and is concluded with a 5 GHz WLAN system demonstration.

During the project, a systematic methodology for power optimization customized to the special features of the target application domain and accompanied by prototype tools is developed. This aims to explore the energy consumed by the embedded processors at the instruction-level, to reduce the power consumption due to data storage and transfer by applying algorithmic transformations, and to implement a power-efficient memory organization and bus interface.

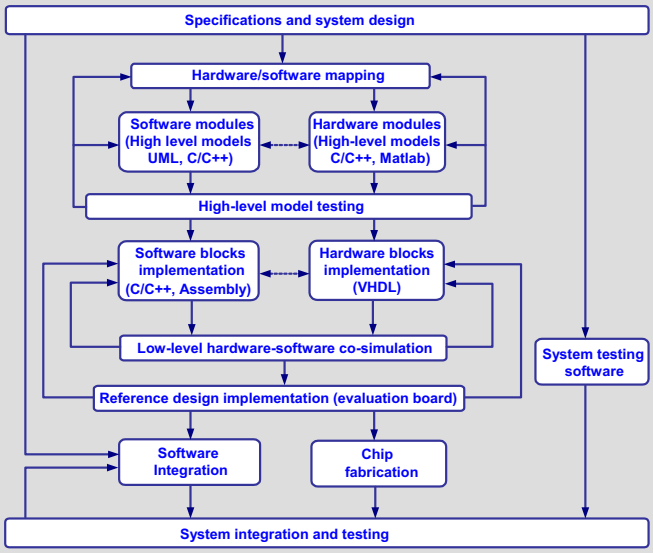
Main project's objectives

- To develop a power-effective heterogeneous SoC, that handles both the baseband processing and the MAC/DLC functionality of the HIPERLAN/2 standard.
  - Flexible architecture to also support IEEE 802.11a critical processing.
- To develop a low-power SoC design methodology for wireless protocol applications, which contains novel power optimization techniques concerning:
  - the system's embedded software
  - the hardware-software mapping procedure
  - the data transfer and storage, and
  - the memory/bus architecture
- To apply the methodology on the SoC design.
- To develop prototype tools based on the low-power design methodology.
- To exploit and disseminate the project's results.

Overview of the design work

- Definition of the wireless system's parameters and requirements.
- Development of a high-level model.
- Definition of the SoC architectural template.
- Hardware-software mapping of the system's functionality.
- Definition of the SoC software architecture and development of the real-time software packages.
- Integration of the software.
- Implementation (design and verification) of the hardware macrocells.
- SoC integration.
- Hardware-software co-simulation and evaluation by a prototype platform.
- SoC fabrication and testing.
- Porting of the software.
- Demonstration of the WLAN 5 GHz system.

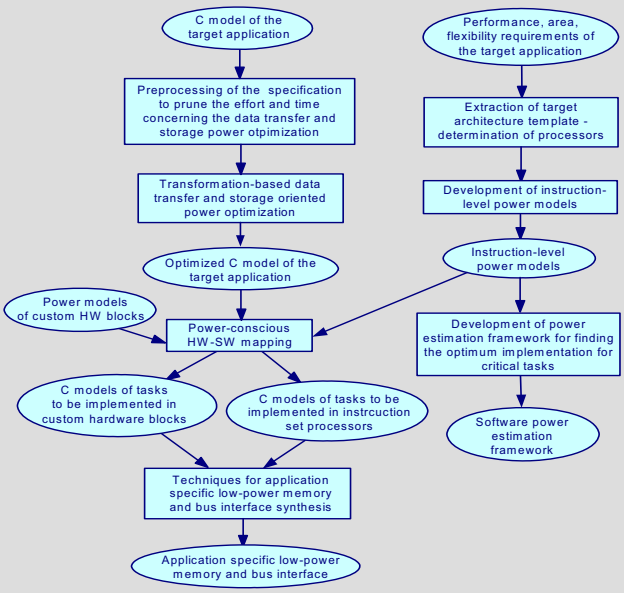
SoC design flow



Low-power methodology

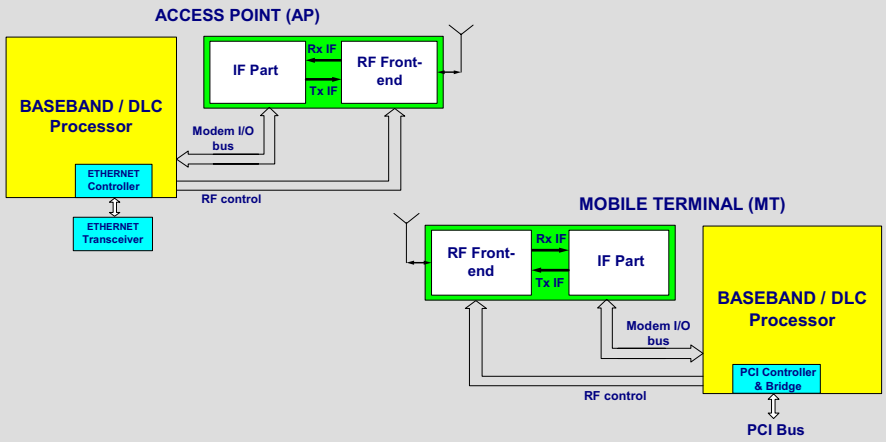
- Preprocessing of the initial specification to prune the effort and time concerning the data transfer and storage power optimization.
- Transformation-based data transfer and storage oriented power optimization.
- Development of a software power estimation framework based on novel instruction-level power models.
- Power-conscious hardware-software mapping of the system's functionality based on hardware and software power models.
- Application-specific low-power memory and bus interface synthesis.
- Prototype tools development for:
  - Preprocessing/pruning of the initial specification.
  - Power-conscious hardware-software mapping.
  - Low-power memory and bus interface synthesis.

Low-power methodology stages



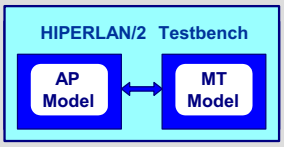
Target development

- The EASY SoC will be suitable for use in a 5 GHz WLAN system that includes an access point and mobile terminals, exchanging Ethernet frames through RF connection.

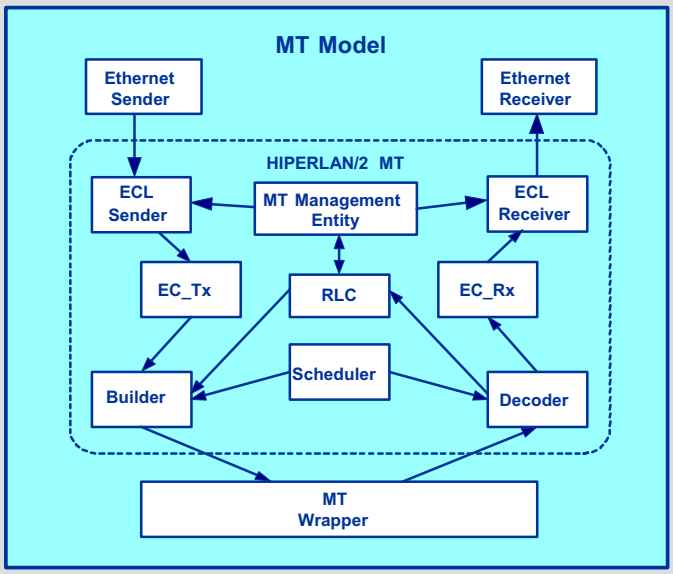


High-level model

- The HIPERLAN/2 application is developed using UML inside the Rational Rose RealTime framework. From the UML-based tool, executable C++ code is produced that is ported to the eCos RTOS for an ARM7TDMI processor.
- The development environment for the HIPERLAN/2 application over eCos was the GNU compiler for the ARM processor, over Windows.
- The execution environment for the HIPERLAN/2 application was the ARMulator instruction set simulator.
- The developed model consists of three major building blocks, the AP model, the MT model and the testbench core module.
- The testbench module is a simple testing environment that creates one AP instance and one MT instance and allows them to transparently exchange Ethernet data.



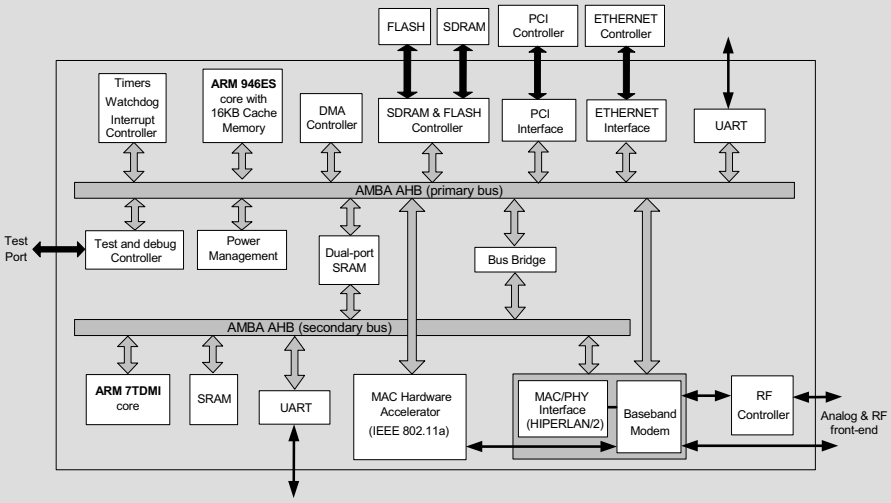
MT model structure



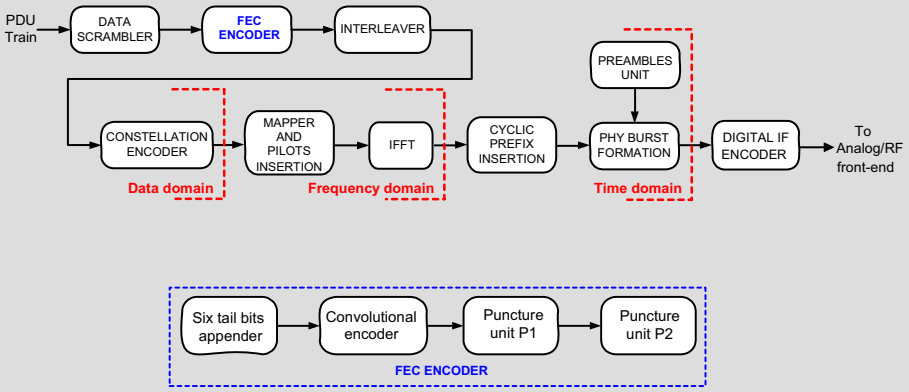
Basic SoC features

- Flexible architecture that is capable to meet the baseband requirements of both HIPERLAN/2 and IEEE 802.11a WLAN standards.
  - OFDM is used as modulation scheme mainly due to its low-cost implementation for frequency selective channels.
- Support the DLC functionality of the HIPERLAN/2 standard and the lower-MAC functionality of the IEEE 802.11a standard.
- Two microprocessor cores: one for protocol processing and a second for modem and lower-MAC control.
- MAC hardware accelerator (custom processor) that implements critical lower-MAC processing of the IEEE 802.11a.
- Various control interfaces (test and debug controller, power controller, Ethernet and PCI interfaces, SDRAM controller, DMA controller, RF controller).
- Low power consumption due to the applied low-power design methodology.

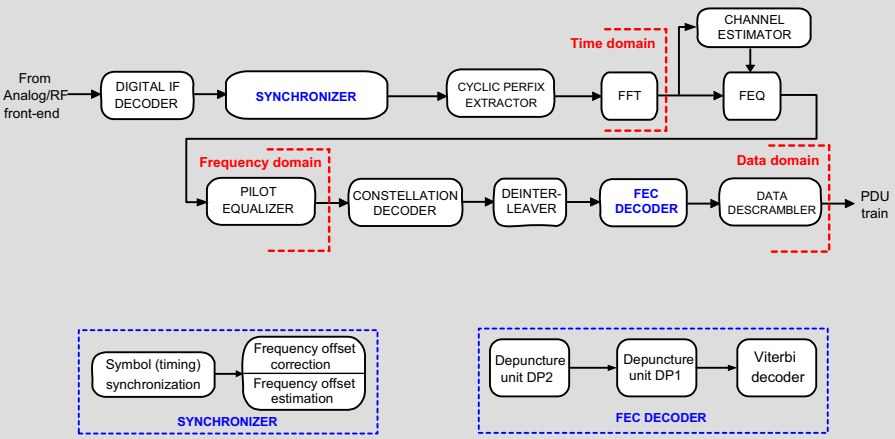
Architectural template



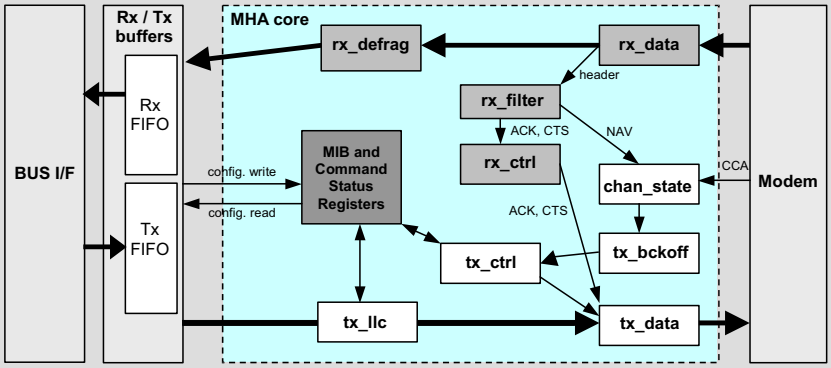
Baseband modem: Transmit path



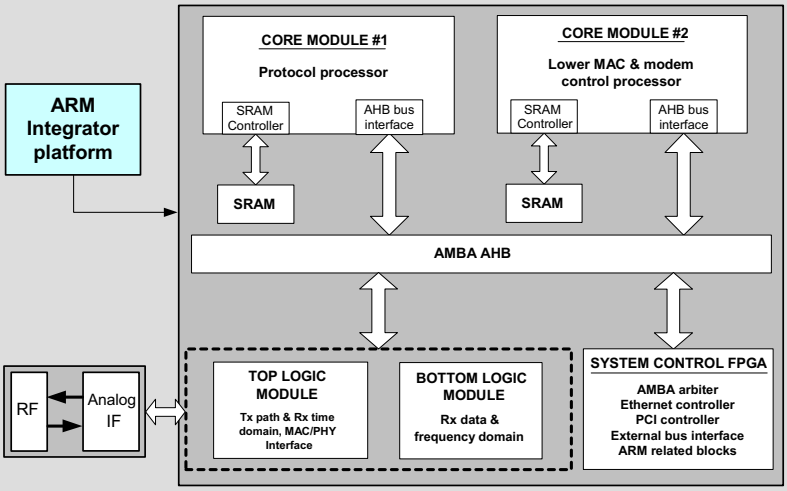
Baseband modem: Receive path



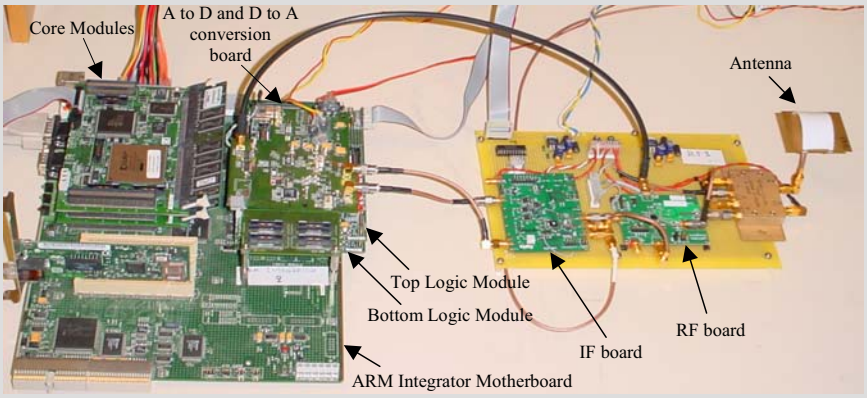
MAC hardware accelerator



FPGA - based prototype (1)



FPGA - based prototype (2)



Demonstration setup

AP - MT system