ANALYTICAL MODELING OF SHORT-CIRCUIT ENERGY DISSIPATION IN SUBMICRON CMOS STRUCTURES

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ABSTRACT

In this paper, an accurate analytical model for the short-circuit energy dissipation of CMOS logic structures, on the basis of a CMOS inverter, is presented. The derived model is based on analytical expressions of the inverter output waveform which include the influences of both transistor currents and the gate-to-drain coupling capacitance. Also, the effect of the short-circuiting transistor's gate-source capacitance on the short-circuit energy dissipation, is taken into account. The α-power law MOS model which considers the carriers' velocity saturation effect of submicron devices, is used. The results produced by the suggested model for a commercial 0.8 μm process show very good agreement with SPICE simulations (error less than 15 % in most cases). After the extension of the inverter model to CMOS gates, the accuracy is maintained at the same level.

1. INTRODUCTION

Energy dissipation in CMOS circuits consists mainly of two parts, the capacitive and the short-circuit energy dissipation. Capacitive dissipation caused by charging and discharging the load capacitance of a CMOS structure is easy to be estimated. During switching in a static CMOS gate, a direct path from the power supply to the ground is established, resulting in short-circuit energy dissipation.

The first closed-form expression for the evaluation of the short-circuit energy dissipation in a CMOS inverter was presented in [1], where zero load capacitance was assumed. This expression gives pessimistic results and is based on the Shichman and Hodges [2] square-law MOS model that ignores the carriers' velocity saturation effects of submicron devices. More recently, in [3] an expression for the short-circuit energy dissipation of the inverter, without the simplifications of [1], was derived. However, the square-law MOS model was used and the expression of the output waveform was derived with negligible short-circuit current.

Sakurai and Newton [4] presented a formula for the short-circuit energy dissipation which is a direct extension of the formula presented in [1]. The only difference is the use of the α-power MOS model for the saturation current expression instead of the square-law model, while all the assumptions of [1] are retained. In [5] a formula for the evaluation of the short-circuit energy dissipation based on the α-power model was proposed, where the analytical expression of the output waveform does not include the influences of the short-circuit current and the gate-to-drain coupling capacitance.

In [6], the short-circuit current waveform was approximated with a piecewise linear function of time, in order to estimate the short-circuit energy dissipation. However, the energy of the reverse current due to the gate-to-drain coupling capacitance is subtracted from the short-circuit energy dissipation. This reverse current is provided from the inverter input, so its energy component cannot be included to the short-circuit energy dissipation, which is due to the direct current from the power supply to the ground. Recently, in [7] a short-circuit energy macromodel for the CMOS inverter was proposed. In this, the short-circuit energy dissipation is evaluated through a short-circuit capacitance. The inverter output is approximated by a linear waveform, based on the inverter propagation delay which is calculated using the empirical timing model proposed in [8].

In this paper, an analytical expression for the evaluation of the short-circuit energy dissipation in a CMOS inverter, based on the α-power law MOS model [4], is derived. For the derivation, analytical expressions of the output waveform in the operation regions which are required for the evaluation of the short-circuit energy dissipation, are used. These expressions take into account the current through both transistors. In order to obtain better accuracy, avoiding an overestimation of the short-circuit energy dissipation, we consider the influence of the input-to-output capacitance and the short-circuiting transistor's gate-source capacitance.

It is important to have an accurate model for the CMOS inverter short-circuit dissipation, since several fast methods for reducing a CMOS gate to an equivalent inverter have been proposed [9],[10]. For the extension of the proposed inverter model to static CMOS gates, the series-connected transistors when operate as charging or discharging block, are reduced to an equivalent transistor using the method proposed in our previous work [10]. Also, a reduction technique for the case where the series-connected transistors operate as the short-circuiting block is used [11].

2. SHORT–CIRCUIT ENERGY DISSIPATION ANALYSIS

The derivations presented in the following are for a rising input ramp: $V_{in} = V_{DD} \cdot (t / \tau)$ for $0 \le t \le \tau$, $V_{in} = 0$ for $t \le 0$ and $V_{in} = V_{DD}$ for $t \ge \tau$, where τ is the input rise time. The analysis for a falling input is symmetrical. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter (Fig.1), taking into account the current through the gate-to-drain coupling capacitance (C_M) is written as

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$$C_L \frac{dV_{out}}{dt} = C_M\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) + I_p - I_n. \quad (1)$$

For the expressions of the transistor currents the four-parameter α-power law MOS model [4] is used. The parameters are the velocity saturation index (α), the drain current (I_{D0}) at $V_{GS}=V_{DS}=V_{DD}$, the drain saturation voltage (V_{D0}) at $V_{GS}=V_{DD}$ and the threshold voltage (V_{TH}). After normalizing voltages with respect to V_{DD}, i.e. $u_{in} = V_{in} / V_{DD}$, $u_{out} = V_{out} / V_{DD}$, $n = V_{THn} / V_{DD}$, $p = |V_{THp}| / V_{DD}$, $u_{don} = V_{Don} / V_{DD}$, $u_{dop} = |V_{Dop}| / V_{DD}$ and using the variable $x = t / \tau$, the PMOS device current is given by the following equation

$$I_p = \begin{cases} k_{lp}(1-x-p)^{\alpha_p/2}(1-u_{out}), & 1-u_{out} < u'_{dop}, \ \textit{Linear} \\ k_{sp}(1-x-p)^{\alpha_p}, & 1-u_{out} \geq u'_{dop}, \ \textit{Saturation} \end{cases} \quad (2)$$

where $k_{sp} = \dfrac{I_{D0p}}{(1-p)^{\alpha_p}}$, $k_{lp} = \dfrac{I_{D0p}}{u_{dop}(1-p)^{\alpha_p/2}}$,

$u'_{dop} = u_{dop}[(1-x-p)/(1-p)]^{\alpha_p/2}$, and the current of the NMOS device in a similar way.

For the evaluation of the short-circuit energy dissipation, analytical expressions of the output waveforms in the two first inverter operation regions (Fig. 2) are required. In region 1 ($0 \leq x \leq n$) the NMOS transistor is off and the PMOS transistor is in the linear region, while in region 2 ($n \leq x \leq x_{satp}$) the NMOS transistor is saturated and the PMOS transistor is still in the linear region. x_{satp} is the normalized time value when the PMOS transistor is entering the saturation region. Part of the charge from the input which injected through the gate-to-drain coupling capacitance causes an overshoot at the early part of the output voltage waveform ($0 \leq x \leq x_1$). During the overshoot there is no current from power supply to ground because the output voltage is greater than the supply voltage. In the special case of very fast input ramps, the PMOS device is turned off after its linear region without enters saturation (Fig.2). This occurs because the output voltage overshoot finishes when the PMOS transistor is already off. In this case there is no short-circuit energy dissipation.

The analytical expressions of the output waveform in the above regions have been derived in our previous work [12], by solving the equation (1) (using some efficient approximations). In region 1, u_{out} is given as

$$u_{out} = 1 + c_m\, y_n^{-1}\left(1 - e^{-y_n x}\right), \quad (3)$$

where $y_n = A_{lp}\left(1 - p - \dfrac{n}{2}\right)^{\alpha_p/2}$, $A_{lp} = \dfrac{k_{lp}\,\tau}{V_{DD}(C_L + C_M)}$

and $c_m = \dfrac{C_M}{C_L + C_M}$.

In region 2 the PMOS current is approximated by a linear function of the normalized time (Fig.3):

$$I_p = I_{pmin} + S\,(x - n).$$

I_{pmin} is calculated using the PMOS current equation in the linear region and the value of the normalized output voltage at $x = n$ in equation (3). The current slope S is calculated by equating the exact PMOS current in the linear region (equation (2)) with the approximated one, at the point $x_c = (1-p) / 2$. After that, the output voltage waveform is described by

$$u_{out} = 1 + c_m(x - n + R) + I_{pmin}\, d\,(x - n) + \frac{S\,d\,(x-n)^2}{2} - \frac{A_{sn}(x-n)^{\alpha_n+1}}{\alpha_n + 1} \quad (4)$$

where $R = y_n^{-1}(1 - e^{-n y_n})$, $d = \tau / V_{DD}(C_L + C_M)$, and

$A_{sn} = \dfrac{k_{sn}\,\tau}{V_{DD}(C_L + C_M)}$.

The normalized time value x_{satp} satisfies the PMOS saturation condition: $u_{out} = 1 - u'_{dop}$. In order to solve this equation a Taylor series expansion around the point $x = 1 - p - n$ up to the second order coefficient is used, for both u_{out} and u'_{dop}. The normalized time value x_1 where the output voltage overshoot finishes is calculated by the equation $u_{out} = 1$, using the Taylor series expansion of u_{out} around the point $x = 2n$. Equations (3), (4) give wave-forms very close to those derived from SPICE simulations (as shown in [12]). Note that, in [5] a rough approximation for x_{satp} is used ($x_{satp} = 1 - p - n$). In [7], a linear output waveform and a constant u'_{dop} are used in order to calculate x_{satp}, and the PMOS transistor current is neglected during the calculation of x_1. The above approximations of previous works result in important errors in the evaluation of the short-circuit dissipation.

The short-circuit energy dissipation for a rising input is the energy of the current (I_{SC}) which provided from the power supply (Fig.1). The inverse current which flows during the interval [0, x_2] (Fig.4) is due to the presence of the gate-drain coupling capacitance (C_M) and the gate-source capacitance of the PMOS transistor (C_{gsp}). The current through these capacitances is provided from the input (or the power supply of the previous gate) during its transition. As shown in Fig.3, the current through C_{gsp} causes a decrease in the positive short-circuit current pulse resulting in reduced short-circuit energy dissipation.

The short-circuit energy dissipation during a falling output transition is defined as

$$E_{SC} = V_{DD}\int_{x_2}^{x_3} I_{SC}\,\tau\,dx = V_{DD}\left(\int_{x_2}^{x_{satp}} I_{SC}\,\tau\,dx + \int_{x_{satp}}^{x_3} I_{SC}\,\tau\,dx\right), \quad (5)$$

where $I_{SC} = I_p - I_{C_{gsp}}$.

The current through C_{gsp} during the input transition is

$$I_{C_{gsp}} = C_{gsp}(dV_{in}/dt) = C_{gsp}(V_{DD}/\tau). \quad (6)$$

In the first integral of (5) a linear approximation of the PMOS transistor current is used (Fig.4)

$$I_p = S'\,(x - x_1). \quad (7)$$

S′ is the slope of I_p and is calculated by equating the exact PMOS current in the linear region (equation (2)) with the approximated one, at the middle of the interval [x_1, x_{satp}]. In the second interval of (5) we use the PMOS saturation current expression of the α-power MOS model (equation (2)). After that, the short-circuit energy dissipation is calculated by the following expression

$$E_{SC} = \frac{V_{DD}\,\tau}{2}\left(x_{satp} - x_2\right)\left[\left(x_{satp} + x_2 - 2x_1\right) S' - \frac{2\,C_{gsp} V_{DD}}{\tau}\right] + \frac{V_{DD}\,k_{sp}\tau}{\left(\alpha_p + 1\right)}\left[\left(1 - p - x_{satp}\right)^{\alpha_p+1} - \left(1 - p - x_3\right)^{\alpha_p+1}\right] - C_{gsp}\,V_{DD}^2\left(x_3 - x_{satp}\right). \quad (8)$$

The value x_2 is the normalized time point where the short-circuit current equals zero, and is easily calculated by the equation

$$S'\left(x_2 - x_1\right) - C_{gsp}\left(V_{DD}/\tau\right) = 0. \quad (9)$$

Similarly, the normalized time value x_3 is calculated by the following equation

$$k_{sp}\left(1 - x - p\right)^{\alpha_p} - C_{gsp}\left(V_{DD}/\tau\right) = 0. \quad (10)$$

The analysis of the short-circuit energy dissipation during the rising output transition is symmetrical.

In order to extend the proposed short-circuit energy dissipation model of the inverter to multiple-input static CMOS gates, the series-connected transistors must be reduced to an equivalent transistor. In our previous work [10], a technique for the reduction of series-connected transistors when they operate as charging or discharging block of a CMOS gate, was presented. The technique is based on the analysis of the dynamic behavior of series-connected transistors, which takes into account the influences of the output load, the inputs' transition time, the body effect, the number and the position of switching inputs and the internal nodes' capacitances. In [11] we developed a reduction method of series-connected transistors when they operate as short-circuiting block in a static CMOS gate. Although, the short-circuiting block has a secondary influence on the gates' output response, it is necessary to analyze its operation in order to achieve an accurate evaluation of the short-circuit energy dissipation in CMOS gates. The channel width of the equivalent transistor in the case of parallel-connected transistors is extracted by adding the channel widths of the switching transistors.

3. RESULTS AND CONCLUSIONS

In Fig.5, the short-circuit energy dissipation during one switching cycle is plotted as a function of the input transition time. A CMOS technology of 0.8μm with V_{DD} = 5V and C_L = 0.2pF, have been used to verify the accuracy of the proposed model. The transistors' widths were: W_n = 4μm, W_p = 6.5μm. Results using the approaches presented in [3],[4],[5] and [7] are also given. Note, that the results from [5] are for C_L = 0, due to the assumption of zero load capacitance in this approach. It can be observed that our model gives results closer to those derived from SPICE simulations than the other methods. The error in most cases is less than 15 %. This occurs because the model includes the influences of the short-circuit current and the gate-to-drain coupling capacitance on the inverter output waveform. Moreover, the effect of the short-circuiting transistor's gate-source capacitance is taken into account. As we can see in Fig.5, the other methods overestimate the short-circuit energy dissipation because they don't include the effects noted above [3],[5], or they use some additional simplifications in order to evaluate the short-circuit energy dissipation [4],[7]. Also, the method used in [3] is based on the square-law MOS model that does not reproduce the current characteristics of short-channel devices well. An important conclusion from the results of Fig.5 is that the contribution of short-circuit energy dissipation to the total dissipation, reaches 40 % for very slow inputs.

In Figures 6 and 7, the short-circuit energy dissipation during one switching cycle for 3 & 4-input NAND gates is plotted as a function of the input transition time, for different combinations of switching inputs. The characteristics of the gates used are: $L_n = L_p$ = 0.8μm, W_n = 8μm, W_p = 4μm, C_L = 0.15pF and V_{DD} = 5V. The curves with the solid and dashed lines have been produced from our analytical model after the application of reduction techniques. The curves with the symbols have been produced from SPICE simulations. The error is maintained at the same level with that of the inverter.

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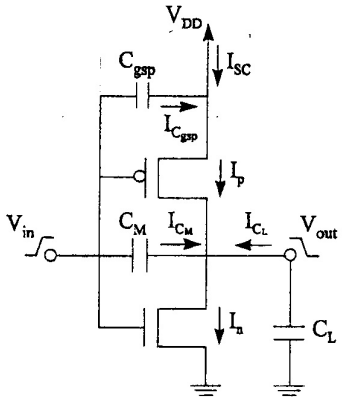

Fig. 1: The CMOS inverter

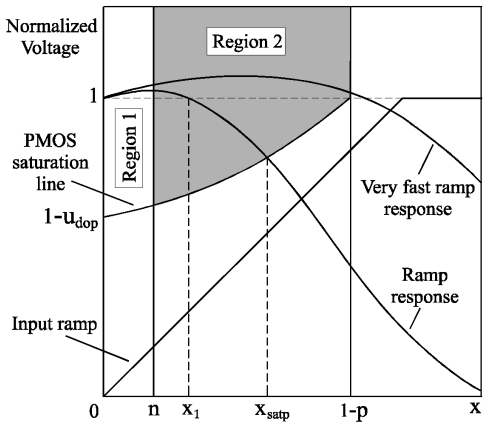

Fig. 2: Operation regions of the inverter

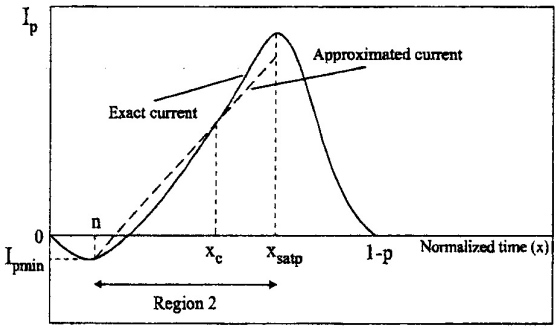

Fig.3: Approximation of the PMOS current in region 2

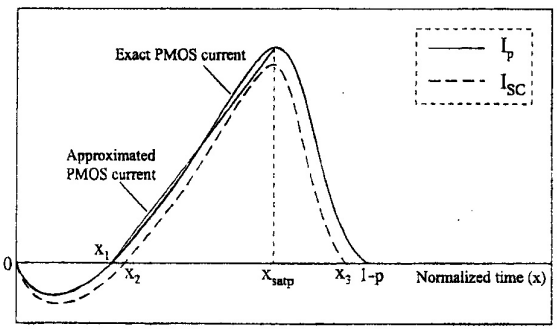

Fig.4: PMOS and short-circuit current waveforms

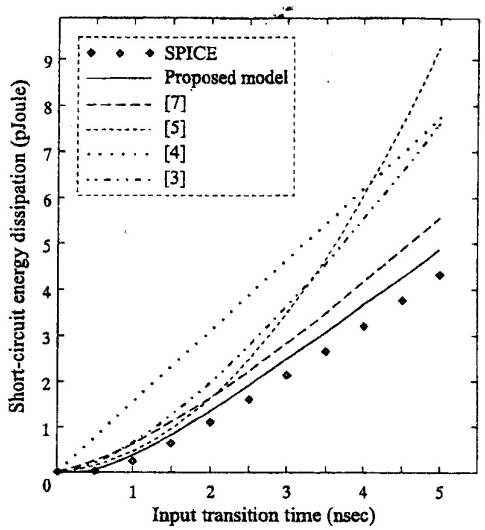

Fig.5: Short-circuit energy dissipation of the inverter during one switching cycle

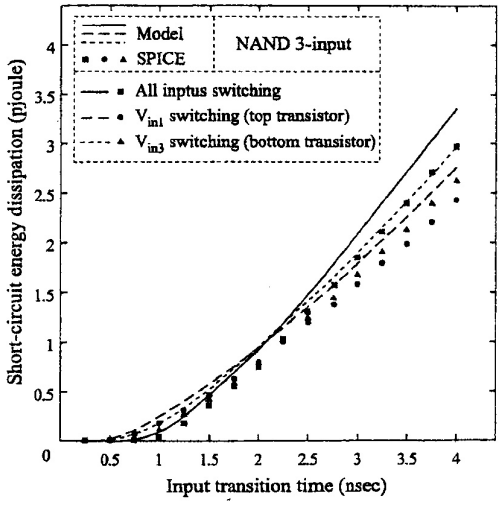

Fig.6: Short-circuit energy dissipation of a 3-input NAND gate during one switching cycle

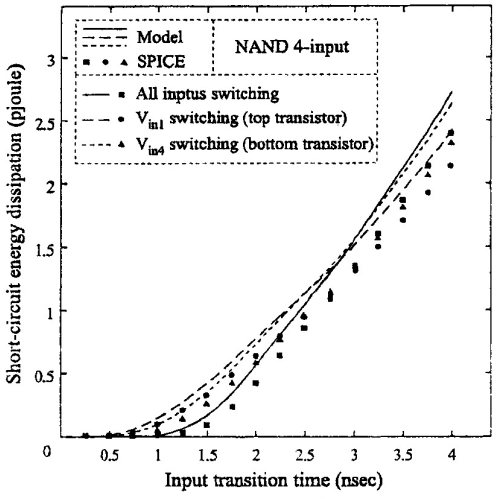

Fig.7: Short-circuit energy dissipation of a 4-input NAND gate during one switching cycle