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INFLUENCE OF THE NMOS AND PMOS TRANSISTOR THRESHOLD VOLTAGES ON CMOS CIRCUITS POWER DISSIPATION

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Abstract: In this paper, the influence of the pMOS and nMOS transistor threshold voltages (V_T) in CMOS digital circuits power dissipation is investigated. It is shown that the difference between the p- and n-channel transistor threshold voltages can be used for reducing the power dissipation. According to the used process silicon technology, lower circuit power reduction is achieving when changes in the circuit are made considering the difference between the pMOS and nMOS threshold voltages. In designs that include Pass Transistor Logic the influence of threshold voltages in power dissipation is studied. As a practical example, a Pass Transistor Logic Full-Adder is analyzed and measurements are given which prove the new idea, suggested in this paper.

I. INTRODUCTION

Threshold voltage (V_T) can be defined as the voltage applied between the gate and the source of an MOS device below which the drain-to-source current effectively drops to zero [1]. The value of the threshold voltage affects the speed of the digital CMOS circuits and their power dissipation [2]. The silicon technology foundries define in their available processes the threshold voltages of the transistor. So, when the designer captures a circuit cannot have any influence in the threshold voltage levels. Although the use of nMOS or pMOS transistor as a pass gate it is in his/her own decision.

In many cases a pass transistor controls the input of a CMOS gate as is shown in Fig.1. When the control signal of the pass transistor is high, the pass transistor is *ON* and the voltage value of its drain passes to the input of the inverter. Then $V_{in} = 0$ when $V_{in\text{-}pass} = 0$, and $V_{in} = V_{DD} - V_{TN}$ when $V_{in\text{-}pass} = V_{DD}$. Otherwise (when the control signal is low) there is no electrical connection between $V_{in\text{-}pass}$ and V_{in}. In case of a pMOS pass transistor (Fig.2) the voltage value of its drain passes to the input of the inverter when the control signal is low. Then $V_{in} = |V_{TP}|$ when $V_{in\text{-}pass} = 0$, and $V_{in} = V_{DD}$ when $V_{in\text{-}pass} = V_{DD}$.

The weakness of V_{in} to be exactly V_{DD} or 0 causes the CMOS gate to have a DC current from V_{DD} to GND. The value of this current depends on the V_{TN} value in case where an nMOS is used as a pass transistor, and on the V_{TP} value in case of a pMOS pass transistor. This current causes power dissipation, which in many applications has a significant contribution in the total power dissipation.

Two methods could be applied to reduce this current.

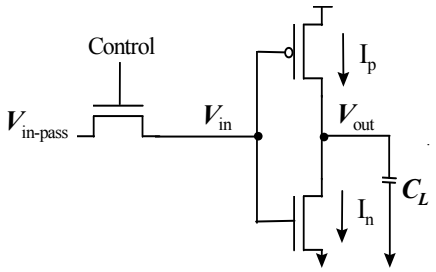

Fig.1:An nMOS pass transistor controls the input of a CMOS inverter

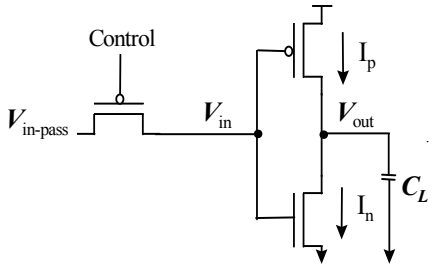

Fig.2:A pMOS pass transistor controls the input of a CMOS inverter

The first one is to apply technology with low threshold voltage for both p and n-channel, and the second one is to implement a circuit properly considering the used technology process. The main disadvantage of the first method is the increase of the delay time of the circuits. The second method, which is proposed in this paper, solves the problem in many cases.

The rest of the paper is organized as follows. Section II studies the influence of both p and n-channel threshold voltages in power dissipation. In section III a new full adder design is compared with the full-adder design presented in [3], as an example of the proposed method for the reduction of the power dissipation. Finally, we conclude in section V.

II. INFLUENCE OF THE THRESHOLD VOLTAGE VALUES IN POWER DISSIPATION

All the chip manufacturers provide processes which are used by the available CAD tools for designing integrated circuits. The circuit designer uses these tools and captures the designs without considering the used technology in the beginning of the design. However, at the simulation phase the technology parameters will be used for the space, time and power calculations. In CMOS technology the values of threshold voltages V_{TN} and V_{TP} of the nMOS and pMOS

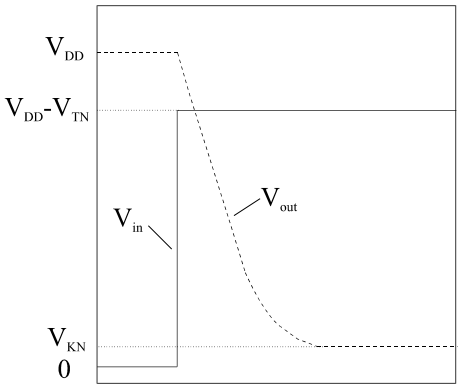

Fig.3:Input and output waveforms for the CMOS inverter of Fig.1

transistor are parameters that the circuit designer can use to meet the timing and power dissipation specifications of the circuit. In the available CMOS technologies there are cases where $|V_{TP}| < V_{TN}$, $|V_{TP}| = V_{TN}$, and $|V_{TP}| > V_{TN}$. The last one is more common than the others.

A popular design logic is the pass transistor logic because of its good characteristics in terms of speed and power dissipation. But, this logic style has the drawback that is explained in the previous section. Fig.3 illustrates the input and the output waveforms of the inverter which is shown in Fig.1 when the control and the drain signals of the pass transistors are high. Due to the weakness of V_{in} to be exactly V_{DD} the pMOS transistor is not turned off. Hence, after the switching of the inverter the output voltage has a value higher than V_{DD} (V_{KN}), resulting in extra power dissipation. In the following, an analysis of the inverter operation in order to calculate this value and show its dependency of the threshold voltages, is presented. For the MOSFET currents, the α-power law model [4] which includes the carriers velocity saturation effect of short-channel devices, is used:

$$I_D = \begin{cases} K_S \left(V_{GS} - V_{TO}\right)^{\alpha}, & V_{DS} \geq V'_{DO}, \quad \textit{Saturation} \\ K_L \left(V_{GS} - V_{TO}\right)^{\alpha/2} V_{DS}, & V_{DS} < V'_{DO}, \quad \textit{Linear} \end{cases}, \quad (1)$$

where $K_S = \dfrac{I_{DO}}{\left(V_{DD} - V_{TO}\right)^{\alpha}}$, $K_L = \dfrac{I_{DO}}{V_{DO}\left(V_{DD} - V_{TO}\right)^{\alpha/2}}$, and $V'_{DO} = V_{DO}\left(\dfrac{V_{GS} - V_{TO}}{V_{DD} - V_{TO}}\right)^{\alpha/2}$.

α is the velocity saturation index, I_{DO} is the drain current at $V_{GS}=V_{DS}=V_{DD}$, V_{DO} is the drain saturation voltage at $V_{GS}=V_{DD}$, and V_{TO} is the zero-bias threshold voltage of the device. According to Fig.1, the input voltage of the inverter is: $V_{in} = V_{DD}-V_{TN}$, where V_{TN} is the threshold voltage of the nMOS pass transistor. Taking into account the body effect, and using an average value for the source voltage of the nMOS pass transistor the threshold voltage is given as

$$V_{TN} = V_{TON} + \gamma \left(\sqrt{2\varphi_F + \frac{V_{DD} - V_{TON}}{2}} - \sqrt{2\varphi_F} \right),$$

where γ is the body effect coefficient and the factor φ_F is the equilibrium Fermi level potential.

In the following we analyze the two regions of the inverter operation. In the first region the nMOS device operates in the saturation region, while in the second one in the linear region. In the analysis it is assumed that the pMOS device is saturated in both regions. This assumption is valid because the pMOS device is in its linear region only for a short period of time at the early part of the inverter switching. The differential equation describing the temporal evolution of the inverter output in the first region, by using the equation (1) for the transistor currents, becomes

$$C_L \frac{dV_{out}}{dt} = -K_{SN}\left(V_{DD} - V_{TN} - V_{TNO}\right)^{\alpha_n} + K_{SP}\left(V_{TN} - |V_{TPO}|\right)^{\alpha_p}. \quad (2)$$

The analytical solution of the above equation is

$$V_{out} = V_{DD} - \frac{K_{SN}\, t}{C_L}\left(V_{DD} - V_{TN} - V_{TNO}\right)^{\alpha_n} + \frac{K_{SP}\, t}{C_L}\left(V_{TN} - |V_{TPO}|\right)^{\alpha_p}. \quad (3)$$

The differential equation in the second region, where the nMOS device operates in its linear region, and the pMOS device is still in its saturation region becomes

$$C_L \frac{dV_{out}}{dt} = -K_{LN}\left(V_{DD} - V_{TN} - V_{TNO}\right)^{\alpha_n/2} V_{out} + K_{SP}\left(V_{TN} - |V_{TPO}|\right)^{\alpha_p}. \quad (4)$$

The analytical solution of (4) is

$$V_{out} = V_{satn} - V_{KN}\, e^{-\frac{K_{LN}}{C_L}\left(V_{DD} - V_{TN} - V_{TNO}\right)^{\alpha_n/2}\left(t - t_{satn}\right)} + V_{KN}$$

where $V_{KN} = \dfrac{K_{SP}\left(V_{TN} - |V_{TPO}|\right)^{\alpha_p}}{K_{LN}\left(V_{DD} - V_{TN} - V_{TNO}\right)^{\alpha_n/2}}$. (5)

V_{satn} is the value of the output voltage when the nMOS device is entering its linear region and t_{satn} is calculated from equation (3), for $V_{out} = V_{satn}$.

The analysis for the case of pMOS pass transistor (Fig.2) is symmetrical. In this case after the switching of the inverter, the output voltage does not reach V_{DD} (Fig.4). The result is extra power dissipation. The difference between the supply voltage and the output voltage is calculated in a similar way and is given by:

$$V_{KP} = \frac{K_{SN}\left(|V_{TP}| - V_{TNO}\right)^{\alpha_n}}{K_{LP}\left(V_{DD} - |V_{TP}| - |V_{TPO}|\right)^{\alpha_p/2}}. \quad (6)$$

Investigating the equations (5) and (6) we get the following conclusions:

- $V_{TNO} > |V_{TPO}| \Rightarrow V_{KP} < V_{KN}$. In this case it is better to use pMOS pass transistor, in order to achieve low power dissipation.
- $V_{TNO} < |V_{TPO}| \Rightarrow V_{KP} > V_{KN}$. In this second case it is better to use nMOS pass transistor.

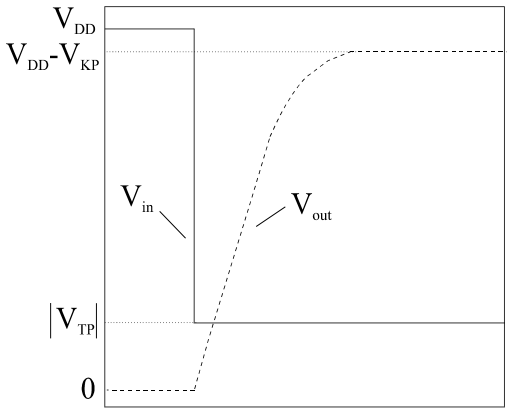

Fig.4:Input and output waveforms for the CMOS inverter of Fig.2

The above conclusions are valid when the used devices are of equal drivabilities ($I_{DON} = I_{DOP}$). Other parameters which can affect the circuit operation are the drain saturation voltage, the body effect parameter and the Fermi level potential of the devices. However, in this paper we analyze the influence of the difference between the device threshold voltages on the circuit operation from the view of the extra power dissipation.

IV. A FULL ADDER EXAMPLE

Because the Full Adder (FA) is the fundamental unit for many arithmetic operations, it is of great importance to design FA circuits that dissipate lower power. Two versions of FAs are analyzed in this paper. The first one given in Fig.5 uses as an input stage an XOR structure [3] and our proposed design (Fig.6) uses as an input stage an XNOR structure [5],[6]. The two designs are almost similar but as is shown below their power dissipation may be varied significant depended of the used technology threshold voltages.

In the first design, the XOR gate output signal has complete values (0 or V_{DD}) when AB=01, 10, 11. But in the case AB = 00, both pMOS devices are *ON* and so the XOR has a poor low level signal (equal to $|V_{TP}|$). In the second design the XNOR gate signal has complete values when AB=00, 01, 10. But in the case AB=11, both nMOS devices are *ON* and so the XNOR has a poor high level signal (equal to $V_{DD}-V_{TN}$).

The two different designs are examined by comparing the SPICE simulation results obtained using the device parameters from two different process technologies. The first one (0.8μm) has $|V_{TPO}| < V_{TNO}$ ($|V_{TPO}| = 0.73$Volts, V_{TNO} = 0.84 Volts) and the second process (1.5μm) has $|V_{TPO}| > V_{TNO}$ ($|V_{TPO}| = 1.1$Volts, $V_{TNO} = 0.7$Volts). The simulation results of the first FA design are shown in Fig.7 for $|V_{TPO}| < V_{TNO}$. In the simulations every 10nsec an input value change is performed resulting in the shown changes of the signals V(XOR) and V(INV-XOR). The worst case occurs when AB=00. The output signal level in XOR structure still can drive the next inverter stage correctly. For the same technology replacing the XOR gate by XNOR gate the output results are illustrated in Fig.8. The worst case occurred when AB=11. The output signal level can not pull-up to V_{DD}, but can still make the next inverter stage work correctly (not so good as the XOR structure). Fig.9 and Fig.10 present the results for the two FA designs by using the second CMOS process technology where $|V_{TPO}| > V_{TNO}$. In this case, the XNOR structure can pull-up and pull-down the input and the output of the CMOS inverter better than the XOR one.

In Fig.11 and Fig.12 the total power consumption of the two FA design schemes are shown. The measurements produce by using the power-meter subcircuit suggested in [7]. The rise and fall times of the input signals are 1nsec. When $|V_{TPO}| < V_{TNO}$ the XOR adder design consumes less power comparing to the XNOR adder design and more when $|V_{TPO}| > V_{TNO}$. So, it is important in low power designs to consider the values of the threshold voltages and choose the proper design according to these values.

V. CONCLUSIONS

In this paper a comparative approach is presented for the influence of the difference between the nMOS and the pMOS threshold voltages, in the total power dissipation. It was shown, by using as an example a full adder cell, that modifications in the circuit design result in reducing the total power consumption without any additional cost in area or delay. Especially in designs with pass transistor logic the easy interchange of nMOS with pMOS transistors, and the opposite, achieves significant reduction of the power dissipation.

VI. REFERENCES

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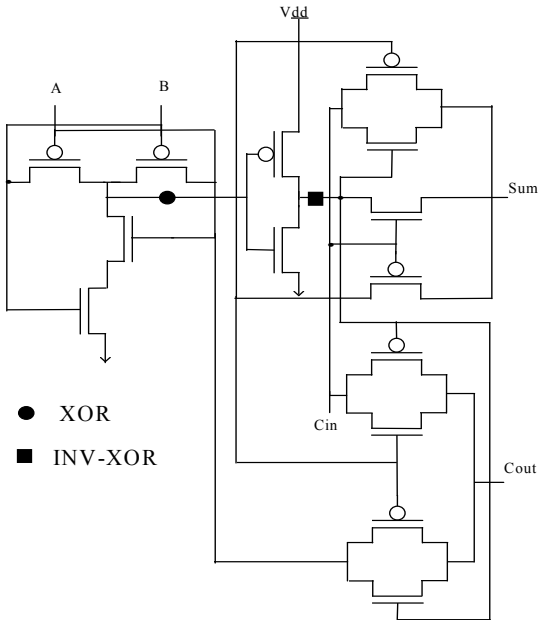

Fig.5:Full-Adder design which uses an XOR gate in its input stage [3]

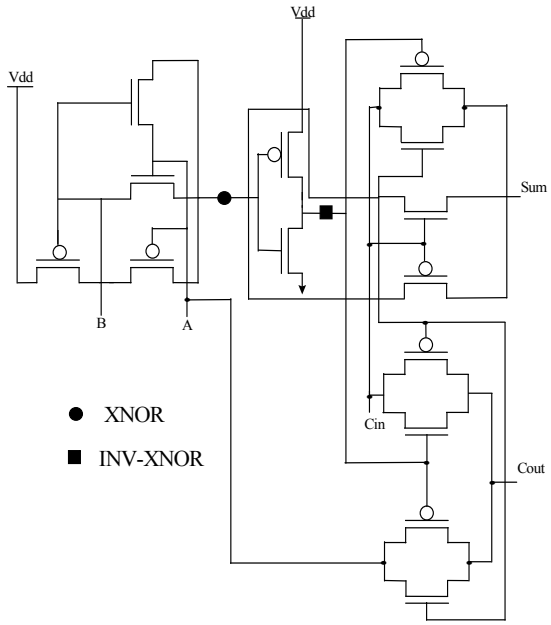

Fig.6:Full-Adder design which uses an XNOR gate in its input stage

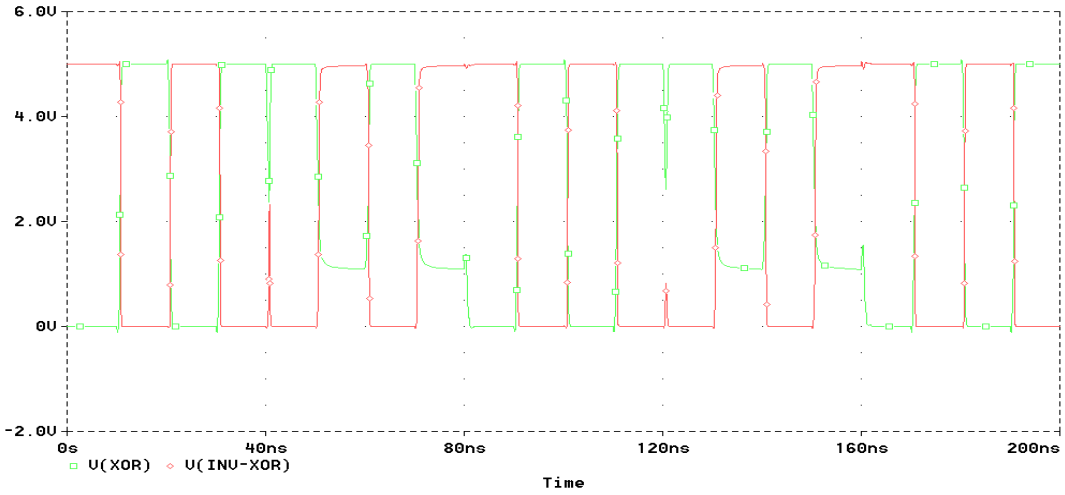

Fig.7: SPICE results for the XOR structure ($|V_{TPO}| < V_{TNO}$)

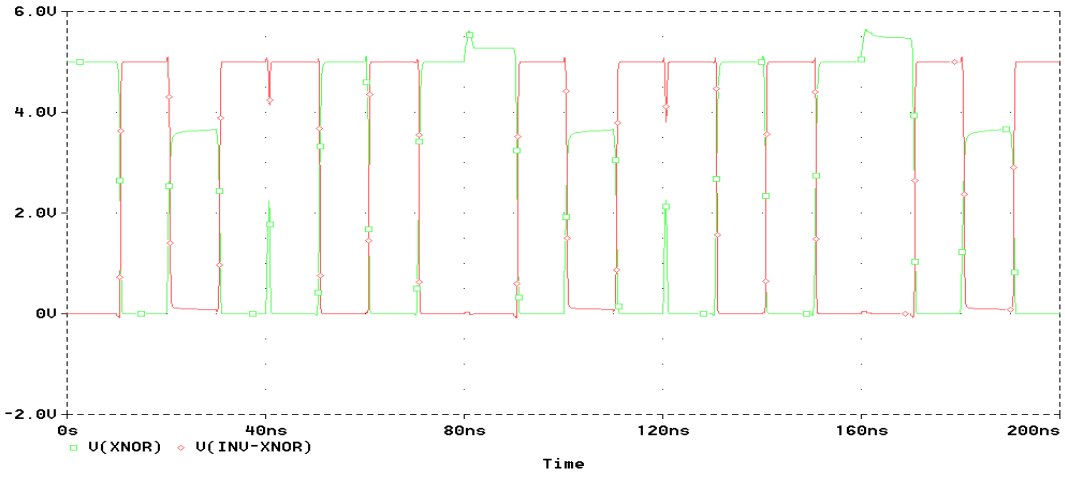

Fig.8: SPICE results for the XNOR structure ($|V_{TPO}| < V_{TNO}$)

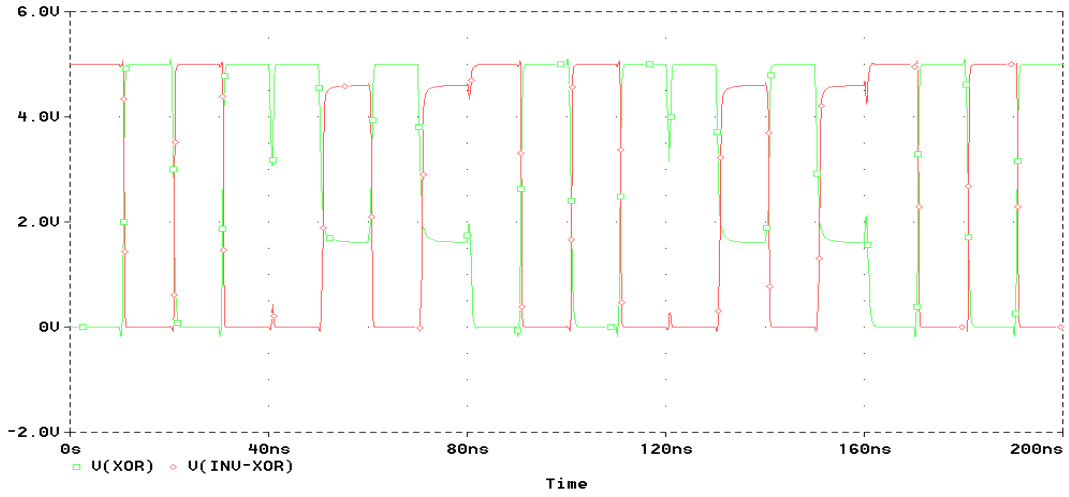

Fig.9: SPICE results for the XOR structure ($|V_{TPO}| > V_{TNO}$)

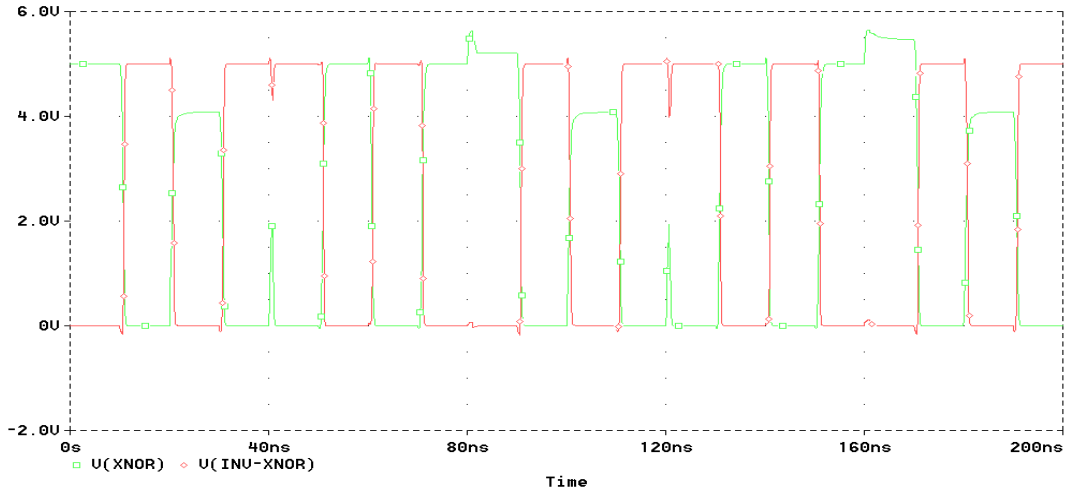

Fig.10: SPICE results for the XNOR structure ($|V_{TPO}| > V_{TNO}$)

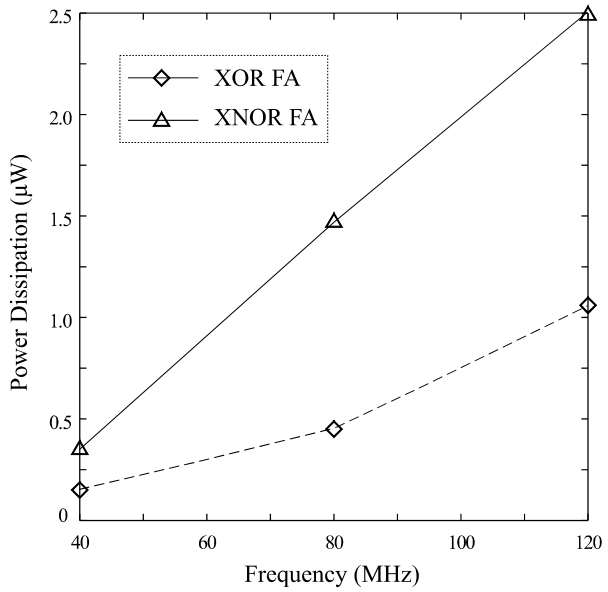

Fig.11: Power dissipation results ($|V_{TPO}| < V_{TNO}$)

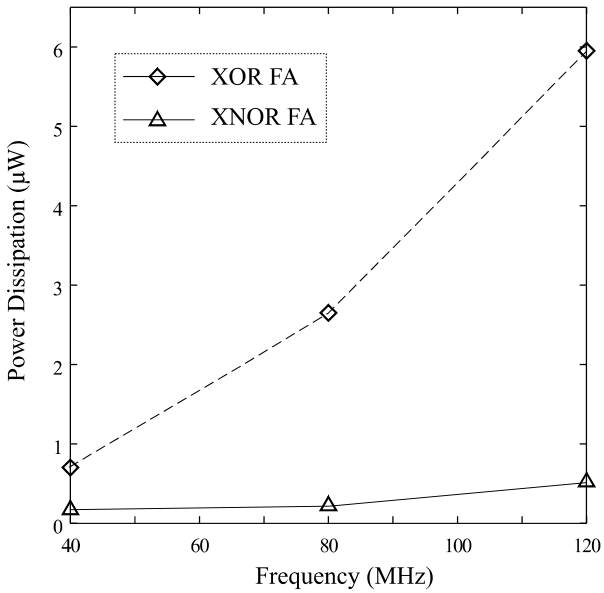

Fig.12: Power dissipation results ($|V_{TPO}| > V_{TNO}$)