CMOS Short-Circuit Power Dissipation Including Velocity Saturation and Gate-to-Drain Capacitive Coupling

L. Bisdounis, S. Nikolaidis[1], O. Koufopavlou

VLSI Design Laboratory, Department of Electrical & Computer Engineering, University of Patras, 26500 Patras, GREECE

[1] Electronics & Computers Division, Department of Physics, University of Thessaloniki, 54006 Thessaloniki, GREECE

E-mail: bisdouni@ee.upatras.gr

ABSTRACT

In this paper an accurate analytical model for the evaluation of the CMOS short-circuit power dissipation, on the basis of a CMOS inverter, is presented. The innovation of the proposed approach against previous works is due to the accurate, analytical expressions of the inverter output waveform which include for the first time the influences of both transistor currents, and the gate-to-drain coupling capacitance. The α-power law MOS model which considers the carriers velocity saturation effects of short-channel devices, is used. The results produced by the suggested model show good agreement with SPICE simulations.

I. INTRODUCTION

Since, power dissipation is one of the most critical parameters in VLSI circuits [1], accurate and efficient power evaluation during the design phase is required in order to meet the power specifications without a costly redesign process. Power dissipation in CMOS circuits consists mainly of two parts, the dynamic and the short-circuit power dissipation. Dynamic dissipation caused by charging and discharging the load capacitance is well understood and easy to be estimated. During the input transition in a static CMOS structure, a direct path from power supply to ground is caused, resulting to short-circuit power dissipation.

The emphasis of this work is on evaluating analytically, the short-circuit power dissipation of a CMOS inverter. To do this, analytical expressions of the output waveform, for the operation regions where short-circuit current exists, must be derived. Analytical expressions for the output waveform including the input slope effects was presented in [2], [3], where the influence of the short-circuit current was neglected. These works are based on the Shichman-Hodges square-law MOS model [4] that ignores the carrier velocity saturation effect. Jeppson [5] presented expressions of the inverter output waveform considering the currents through both transistors, but still based on the square-law MOS model. Sakurai and Newton [6], [7] introduced the α-power (n-power in [7]) law MOS model that considers of the velocity saturation effect, which becomes prominent in short-channel devices, and they presented analytical expressions for the inverter output waveform. However, in [6] the short-circuit current is neglected, while in [7] a fictitious input ramp is used in order to approximate the

CMOS inverter by a NMOS circuit. This approximation is exact only for extreme cases of input ramps, and does not model accurately the early part of the inverter output waveform, where short-circuit power is dissipated.

The first closed-form expression for the evaluation of the short-circuit power dissipation in a CMOS inverter was presented in [8] where zero load capacitance, and current waveform which is mirror symmetric about a central vertical axis (at the half of the input transition time), were considered. This expression gives the maximum value of the short-circuit power dissipation, and is based on the square-law MOS model. More recently, in [2], [9] an expression for the short-circuit energy dissipation of the CMOS inverter, without the simplifications of [8], was derived. However, as mentioned above, the square-law MOS model was used, and the expression of the output waveform was derived with negligible short-circuit current.

Sakurai and Newton [6] presented a formula for the short-circuit energy dissipation during one switching cycle, which is a direct extension of the formula presented in [8]. The only difference is the use of the α-power MOS model for the expression of the saturation current, instead of the square-law MOS model, while all the assumptions of [8] are remained. Vemuru and Scheinberg [10] proposed a formula for the evaluation of the short-circuit power dissipation, based on the α-power MOS model, where the analytical expression of the output waveform used, doesn't include the influences of the short-circuit current, and the gate-to-drain coupling capacitance. A formulation of the short-circuit power dissipation through an equivalent short-circuit capacitance with no physical mean is presented in [11], where mean charge conservation across the CMOS structure, and a linear rough approximation of the output waveform, are used.

In this work, an analytical expression for the evaluation of the short-circuit power dissipation in a CMOS inverter, based on the α-power law MOS model [6] which includes the carries velocity saturation effects of short-channel devices, is derived. For the derivation, analytical expressions of the output waveform, which considers the current through both transistors, are used. In order to obtain better accuracy, avoiding an overestimation of the short-circuit power dissipation, the influence of the gate-to-drain coupling capacitance, is considered. The presented expression shows the influence of the inverter design characteristics, the load capacitance, and the slope of the input waveform driving the inverter, on the short-circuit power dissipation.

II. INVERTER OUTPUT WAVEFORM ANALYSIS

The inverter input voltage is assumed to be a pulse. The pulse edges are given by,

$$V_{in} = \begin{cases} \dfrac{V_{DD}\, t}{\tau_r}, & \text{rising input} \\ V_{DD}\left(1 - \dfrac{t}{\tau_f}\right), & \text{falling input} \end{cases} \tag{1}$$

where τ_r, τ_f are the input rise and fall times, respectively. The expressions of the output waveform presented in the following are for the rising input edge. The analysis for the falling input edge is symmetrical.

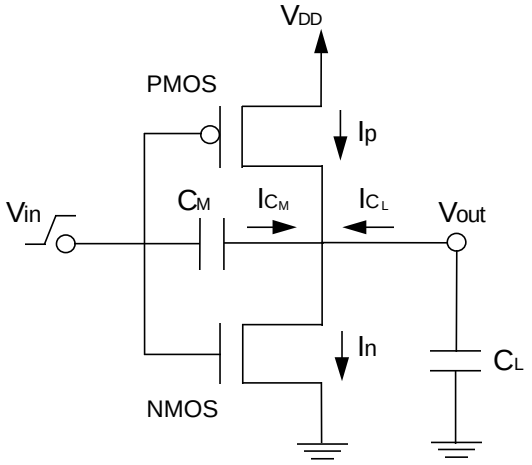


Fig.1: The CMOS inverter

The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter of Fig.1, taking into account the gate-drain capacitive coupling (C_M) [12], is derived from the application of the Kirchoff's current law to the output node,

$$I_{C_L} + I_{C_M} + I_p - I_n = 0\,,$$

$$C_L \frac{dV_{out}}{dt} = C_M\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) + I_p - I_n\,. \qquad (2)$$

For the expressions of the transistors current the four-parameter α-power MOS model, is used. The parameters are the velocity saturation index (α), the drain current (I_{D0}) at V_{GS}=V_{DS}=V_{DD}, the drain saturation voltage (V_{D0}) at V_{GS}=V_{DD}, and the threshold voltage (V_{TH}). After normalizing the voltages with respect to V_{DD}, i.e. $u_{in} = V_{in} / V_{DD}$, $u_{out} = V_{out} / V_{DD}$, $n = V_{THn} / V_{DD}$, $p = |V_{THp}| / V_{DD}$, $u_{don} = V_{D0n} / V_{DD}$, $u_{dop} = V_{D0p} / V_{DD}$, and using the variable $x = t / \tau_r$, the NMOS, PMOS device currents [6] of the CMOS inverter are given by the following equations,

$$I_n = \begin{cases} 0\,, & x \le n\,, & \text{Cutoff region} \\ k_{sn}(x-n)^{\alpha_n}\,, & u_{out} \ge u'_{don}\,, & \text{Saturation region}\,, \\ k_{ln}(x-n)^{\alpha_n/2}\,u_{out}\,, & u_{out} < u'_{don}\,, & \text{Linear region} \end{cases} \qquad (3)$$

where, $k_{sn} = \dfrac{I_{D0n}}{(1-n)^{\alpha_n}}$, $k_{ln} = \dfrac{I_{D0n}}{u_{don}(1-n)^{\alpha_n/2}}$, and $u'_{don} = u_{don}\left(\dfrac{x-n}{1-n}\right)^{\frac{\alpha_n}{2}}$,

$$I_p = \begin{cases} k_{lp}(1-x-p)^{\alpha_p/2}(1-u_{out}), & 1-u_{out} < u'_{dop}, \quad \text{Linear region} \\ k_{sp}(1-x-p)^{\alpha_p}, & 1-u_{out} \geq u'_{dop}, \quad \text{Saturation region}, \\ 0, & x \geq 1-p, \quad \text{Cutoff region} \end{cases} \tag{4}$$

where, $k_{sp} = \dfrac{I_{D0p}}{(1-p)^{\alpha_p}}$, $k_{lp} = \dfrac{I_{D0p}}{u_{dop}(1-p)^{\alpha_p/2}}$, and $u'_{dop} = u_{dop}\left(\dfrac{1-x-p}{1-p}\right)^{\frac{\alpha_p}{2}}$.

Short-circuit power is dissipated when a direct current path from power supply to ground occurs. Due to the current through the input-to-output coupling capacitance (C_M), an overshoot occurs at the early part of the output voltage waveform (Fig. 2). During the overshoot there is no current from power supply to ground because V_{out} is higher than V_{DD}. Thus, short-circuit power is dissipated from the end of the output voltage overshoot ($x = x_1$), until the PMOS device is turned off ($x = 1 - p$). If we consider input ramps such that the NMOS device is still saturated when the input voltage ramp reaches the value $V_{DD} - |V_{TP}|$, which holds for the most practical cases in VLSI circuits, then we analyze the three first operation regions (Fig.2) of the inverter in order to evaluate the short-circuit power dissipation.

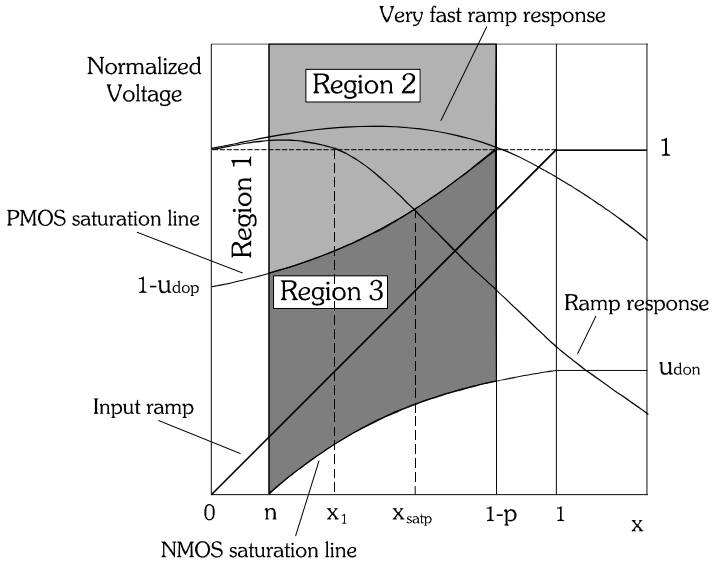


Fig.2: Operation regions of the inverter

Region 1, $0 \leq x \leq n$: The PMOS transistor is in the linear region. Since, the NMOS transistor is off the discharge of the output node does not start in this region, which means that the end of the output voltage overshoot occurs in the next region. Thus, in this region there is no short-circuit power dissipation, but the expression of the output voltage waveform is required, in order to find the initial conditions of the next region. The differential equation (2), using the current equations (3), (4) becomes,

$$\frac{du_{out}}{dx} = c_m + A_{lp}(1-x-p)^{\alpha_p/2}(1-u_{out}), \tag{5}$$

where, $c_m = \frac{C_M}{C_L + C_M}$, and $A_{lp} = \frac{k_{lp}\,\tau_r}{V_{DD}(C_L + C_M)}$. The first term of the right part in (5) corresponds to the charging current through the coupling capacitance (C_M), which causes the major influence on the output voltage waveform in this region. Since, the above differential equation cannot be solved analytically, an average value of x (x_{av} = n / 2) is used in the expression of the PMOS current, resulting in an approximation solution of (5),

$$u_{out} = 1 + c_m\, y_n^{-1}\left(1 - e^{-y_n x}\right), \tag{6}$$

where, $y_n = A_{lp}\left(1 - p - \frac{n}{2}\right)^{\frac{\alpha_p}{2}}$.

Region 2, $n \le x \le x_{satp}$: The NMOS device is saturated and the PMOS device is still in the linear region. Note, that the right limit of this region is the normalized time value x_{satp} (Fig.2) where the PMOS device enters saturation, i.e. 1 - u_{out} = u'_{dop} . As we can see in Fig.2, in the special case of very fast input ramps, the PMOS device is turned off after its linear region, without enters saturation. In this region, the differential equation (2) becomes,

$$\frac{du_{out}}{dx} = c_m - A_{sn}(x-n)^{\alpha_n} + A_{lp}(1-x-p)^{\alpha_p/2}(1-u_{out}), \tag{7}$$

where, $A_{sn} = \frac{k_{sn}\,\tau_r}{V_{DD}(C_L + C_M)}$. The third term of the right part in (7) corresponds to the PMOS device current. Since, the influence of the PMOS current on the output voltage waveform is small, two approximations concerning this term are used, in order to give a solution of (7). First, an approximation of u_{out} in the expression of the PMOS current is used. The approximated u'_{out} is derived assuming negligible PMOS current in (7),

$$u'_{out} = 1 + c_m(x-n+R) - \frac{A_{sn}}{(\alpha_n+1)}(x-n)^{\alpha_n+1},$$

where $R = y_n^{-1}\left(1 - e^{-n y_n}\right)$. Second, a constant value of x (x_c = 0.9 (1- p)) in the normalized gate-source voltage of the PMOS device has be found, to compensate the error of the underestimated u'_{out}. After the above approximations, the solution of (7) is,

$$\begin{aligned} u_{out} = {} & 1 + c_m(R-n)(1+n\,y_s) + \frac{c_m\, y_s\, n^2}{2} + c_m\left[1 - y_s(R-n)\right]x \\ & - \frac{c_m\, y_s\, x^2}{2} + \frac{A_{sn}(x-n)^{\alpha_n+1}}{(\alpha_n+1)}\left[\frac{(x-n)\,y_s}{(\alpha_n+2)} - 1\right] \end{aligned}, \tag{8}$$

where, $y_s = A_{lp}\left[0.1\,(1-p)\right]^{\alpha_p/2}$. The above equation gives waveforms very close to those derived from SPICE simulations, which indicates the validation of the above approximations.

In order to continue the analysis for the next region, the evaluation of the normalized time value x_{satp} and the normalized output voltage value u_{satp}, where the PMOS device saturates, is required. These values satisfy the PMOS saturation condition: $u_{out} = 1 - u'_{dop}$. In order to solve this equation a Taylor series expansion at the point x = 1 - p - n, up to the fourth order coefficient is used, for both u_{out}, u'_{dop}. After that, the PMOS saturation condition becomes,

$$\sum_{k=0}^{4} z_k x^k = 1 - \sum_{k=0}^{4} m_k x^k \,, \tag{9}$$

where z_k, m_k are the Taylor series coefficients. Standard ways of evaluating these coefficients can be found in most mathematical handbooks. The solution of (9) which exists in the interval [n, 1-p], is x_{satp}. The error, which is inserted in the evaluation of x_{satp}, due to the above method is up to 0.3%. By substituting x_{satp} in equation (8) the normalized output voltage u_{satp}, is evaluated. Note, that in [10] a rough approximation for x_{satp} is used (x_{satp} = 1 - n - p), which results to an important error in the evaluation of the short-circuit power dissipation. Another way with lower computational complexity, in order to evaluate x_{satp}, is the use of the empirical coefficient *b*, so that $x_{satp} = b\,(1 - n - p)$. In order to determine the values of *b*, a single lumped parameter $G_{n1} = (I_{D0n}\,\tau_r) / [V_{DD}\,(C_L + C_M)]$ which takes into account the input waveform slope, the drive of the switching transistor and the output, gate-to-drain capacitances, is introduced. In the following table, the values of *b* depending on the parameter G_{n1}, are given. Note, that for $G_{n1} < 0.25$, the PMOS device is turned off after its linear region (very fast input ramps). In this case there is no short-circuit power dissipation.

G_{n1}	0.25 - 0.4	0.4 - 0.6	0.6 - 1	1 - 1.8	1.8 - 3	> 3
b	1.20	1.15	1.10	1.0	0.95	0.85

Table I: Empirical coefficient (*b*) for the evaluation of x_{satp}.

Region 3, $x_{satp} \le x \le 1\text{-}p$: Both transistors are saturated. The differential equation (2) becomes:

$$\frac{du_{out}}{dx} = c_m - A_{sn}(x-n)^{\alpha_n} + A_{sp}(1-x-p)^{\alpha_p} \,, \tag{10}$$

where, $A_{sp} = \dfrac{k_{sp}\,\tau_r}{V_{DD}(C_L + C_M)}$. The analytical solution of equation (10) is,

$$u_{out} = u_{23} + c_m x - \frac{A_{sn}}{(\alpha_n + 1)}(x-n)^{\alpha_n+1} - \frac{A_{sp}}{(\alpha_p + 1)}(1-x-p)^{\alpha_p+1} \tag{11}$$

where the integration constant which is inserted to ensure continuity with respect to region 2, is given by,

$$u_{23} = u_{satp} - c_m x_{satp} + \frac{A_{sn}}{(\alpha_n + 1)}\left(x_{satp} - n\right)^{\alpha_n + 1} + \frac{A_{sp}}{(\alpha_p + 1)}\left(1 - x_{satp} - p\right)^{\alpha_p + 1}$$

where (x_{satp} , u_{satp}) is the starting point of region 3.

III. CMOS SHORT-CIRCUIT POWER DISSIPATION

As mentioned in section II, during the overshoot of the output voltage waveform there is no current from power supply to ground because V_{out} is higher than V_{DD}. Thus, short-circuit energy is dissipated from the end of the overshoot ($x=x_1$), until the PMOS device is turned off ($x=1-p$). The short-circuit energy dissipation during a falling output transition, is given by,

$$E_{SCF} = V_{DD} \int I_{SC}\, dt = V_{DD} \int_{x_1}^{1-p} I_p\, \tau_r\, dx\,. \tag{12}$$

The assumption that, the NMOS device is still saturated when the input voltage ramp reaches the value $V_{DD} - |V_{TP}|$ i.e. $x=1-p$, holds for the cases where $G_{n1} < 4$, which is true for the most practical conditions in VLSI circuits. The application of the Kirchoff's current law to the output node of the inverter (2) is then written as,

$$I_p = k_{sn}(x - n)^{\alpha_n} - \frac{V_{DD} C_M}{\tau_r} + \frac{V_{DD}(C_M + C_L)}{\tau_r}\,\frac{du_{out}}{dx} \tag{13}$$

The integration of (12) using (13) yields,

$$E_{SCF} = \frac{V_{DD}\, k_{sn}\, \tau_r}{(\alpha_n + 1)}\left[(1 - p - n)^{\alpha_n + 1} - (x_1 - n)^{\alpha_n + 1}\right] - V_{DD}^2 C_M (1 - p - x_1) + V_{DD}^2 (C_L + C_M)\left(u_{[1-p]} - 1\right), \tag{14}$$

where x_1 is the normalized time value in which the end of the output voltage overshoot occurs, and $u_{[1-p]}$ is the value of the normalized output voltage when the PMOS device is turned off, and is evaluated from equation (11) for $x = 1 - p$,

$$u_{[1-p]} = u_{23} + c_m(1 - p) - \frac{A_{sn}}{(\alpha_n + 1)}(1 - p - n)^{\alpha_n + 1}\,.$$

The end of the output voltage overshoot occurs in region 2, due to the fact that the discharge of the output node, which is initially charged at V_{DD}, doesn't start in region 1 since the NMOS device is off. Thus, x_1 is evaluated if we set $u_{out} = 1$ in equation (8). As in the case of x_{satp} (section II - region 2), a Taylor series expansion of u_{out} but in this case at the point 2n, is

used. This results to an error in the evaluation of x_1 up to 0.1%. Furthermore, an empirical coefficient *q*, so that $x_1 = q\ (2n)$, can be used. The values of *q* depending on the single parameter $G_{n2} = (I_{D0n}\ \tau_r) / (V_{DD}\ C_M)$ which takes into account the input waveform slope, the drive of the switching transistor and the gate-to-drain coupling capacitance, are given in Table II. Note, that for $G_{n2} < 6$, the PMOS device is turned off after its linear region.

G_{n2}	6 - 8	8 - 10	10 - 14	14 - 20	20 - 30	30 - 45	> 45
q	2.05	1.75	1.50	1.30	1.05	0.90	0.80

Table II: Empirical coefficient (*q*) for the evaluation of x_1 .

Note, that the analysis in order to evaluate the short-circuit energy dissipation during the rising output transition is symmetrical, and results to the following formula,

$$E_{SCR} = \frac{V_{DD}\, k_{sp}\, \tau_f}{(\alpha_p + 1)} \left[(1 - n - p)^{\alpha_p + 1} - (x_1 - p)^{\alpha_p + 1} \right] - V_{DD}^2 C_M (1 - n - x_1) - V_{DD}^2 (C_L + C_M)\, u_{[1-n]} \quad , \tag{15}$$

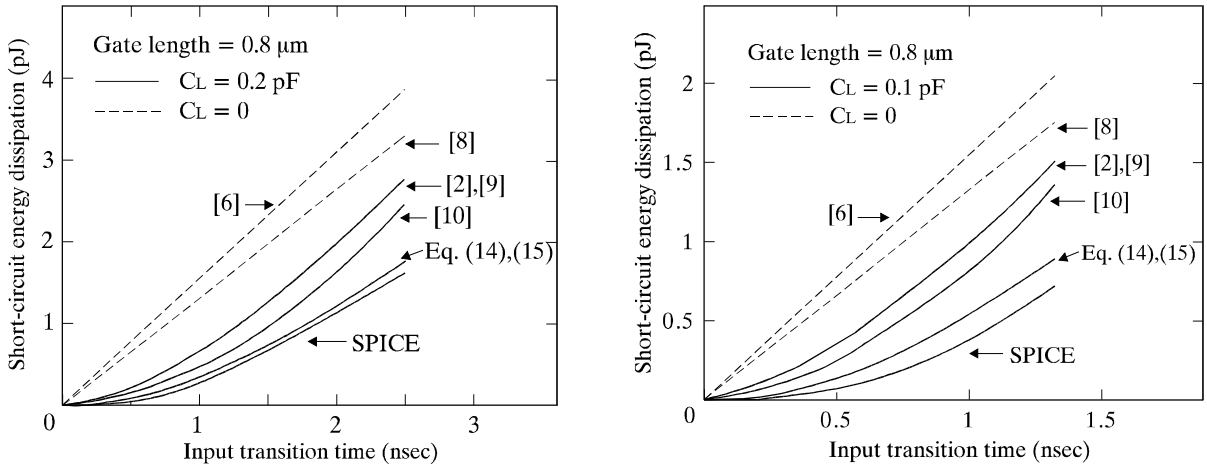
where x_1 is now the normalized time value in which the end of the output voltage undershoot occurs, and $u_{[1\text{-}n]}$ is the value of the normalized output voltage when the NMOS device is turned off. Finally, the short-circuit power dissipation P_{SC} is given by:

$$P_{SC} = (E_{SCF} + E_{SCR})\ f\ , \tag{16}$$

where f is the switching frequency.

In Fig.3, the short-circuit energy dissipation during one switching cycle, is plotted as a function of the input transition time. The results have been derived, for an inverter with equal NMOS and PMOS gate lengths $L_n = L_p = 0.8\mu m$, and $W_n = 4\mu m$, $W_p = 6.55\mu m$ in order to achieve equal drain currents at $V_{GS} = V_{DS} = V_{DD}$ ($I_{D0n} = I_{D0p} = 1.72$ mA), $n = 0.17$, and $p = 0.15$. A supply voltage of 5Volts, an output load of 0.2pF (Fig.3a) and 0.1pF (Fig.3b), and the values $C_M = 9.4$fF (for rising input), $C_M = 7.2$fF (for falling input), were used. The values of the velocity saturation indexes were $\alpha_n = 1.29$ and $\alpha_p = 1.41$, and the saturation voltages at $V_{GS} = V_{DD}$ were $V_{D0n} = 1.75$Volts and $V_{D0p} = 2.35$Volts. The SPICE simulations have been obtained by using the powermeter subcircuit proposed in [13],[14] for the parameters of a 0.8 micron process technology. Also, results using the approaches for the evaluation of the short-circuit energy dissipation presented in [2], [9], [6], [8], [10], are given. Note, that the results from [6], [8] are for $C_L = 0$, due to the assumption of zero load capacitance in these approaches. It can be observed, that the presented model gives results closer to those derived from SPICE simulations than the other methods. This occurs because our model includes the

influences of the short-circuit current, and the gate-to-drain coupling capacitance on the expression of the inverter output waveform. Also, a quite accurate method is used for the determination of the time where the short-circuiting transistor changes from the linear region to the saturation region.



(a) Output load = 0.2 pF (b) Output load = 0.1 pF

Fig.3: Short-circuit energy dissipation of a CMOS inverter per one clock cycle

IV. CONCLUSION

In this paper an accurate model for the evaluation of the CMOS short-circuit power dissipation, is presented. The model is based on accurate expressions for the inverter output waveform, which take into account the influences of both transistor currents, and the gate-to-drain coupling capacitance. Also, the velocity saturation effects of short-channel devices are included. The comparison of the results produced by the proposed approach with previous works, shows better agreement with SPICE measurements.

REFERENCES

[1] A.P. Chandrakasan, S. Sheng, and R.W. Brodersen, “Low-power CMOS digital design”, *IEEE J. Solid-State Circuits*, vol. 27, pp. 473-484, April 1992.

[2] N. Hedenstierna, K.O. Jeppson, “CMOS circuit speed & buffer optimization”, *IEEE Trans. Computer-Aided Design*, vol. CAD-6, pp. 270-281, March 1987.

[3] A.I. Kayssi, K.A. Sakallah, and T.M. Burks, “Analytical transient response of CMOS inverters”, *IEEE Trans. Circuits and Systems-I*, vol. 39, pp. 42-45, January 1992.

[4] H. Shichman and D.A. Hodges, “Modeling and simulation of insulated-gate field-effect transistor switching circuits”, *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 285-289, September 1968.

[5] K.O. Jeppson, “Modeling the influence of the transistor gain ratio, and the input-to-output coupling capacitance on the CMOS inverter delay”, *IEEE J. Solid-State Circuits*, vol. 29, pp. 646-654, June 1994.

[6] T. Sakurai, A.R. Newton, “Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas”, *IEEE J. Solid-State Circuits*, vol. 25, pp. 584-594, April 1990.

[7] T. Sakurai, A.R. Newton, “A simple MOSFET model for circuit analysis”, *IEEE Trans. Electron Devices*, vol. 38, pp. 887-894, April 1991.

[8] H.J.M. Veendrick, “Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits”, *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 468-473, August 1984.

[9] N. Hedenstierna, K.O. Jeppson, “Comments on ‘A module generator for optimized CMOS buffers’ ”, *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 180-181, January 1993.

[10] S.R. Vemuru, N. Scheinberg, “Short-circuit power dissipation estimation for CMOS logic gates”, *IEEE Trans. Circuits and Systems-I*, vol. 41, pp. 762-765, November 1994.

[11] S. Turgis, N. Azemard, and D. Auvergne, “Explicit evaluation of short-circuit power dissipation for CMOS logic structures”, in *Proc. Inter. Symposium on Low-Power Design*, pp. 129-134, April 1995.

[12] M. Shoji, *CMOS Digital Circuit Technology*. New Jersey: Prentice-Hall, 1987.

[13] S.M. Kang, “Accurate simulation of power dissipation in VLSI circuits”, *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 889-891, October 1986.

[14] G.Y. Yacoub, W.H. Ku, “An enhanced technique for simulating short-circuit power dissipation”, *IEEE J. Solid-State Circuits*, vol. 24, pp. 844-847, June 1989.