MODELING THE CMOS SHORT-CIRCUIT POWER DISSIPATION

L. Bisdounis[1], S. Nikolaidis[2], O. Koufopavlou[1]*, C.E. Goutis[1]

[1] VLSI Design Laboratory, Department of Electrical & Computer Engineering, University of Patras, 26110 Patras, GREECE

[2] Electronics & Computers Division, Department of Physics, University of Thessaloniki, 54006 Thessaloniki, GREECE

E-mail: bisdouni@ee.upatras.gr

ABSTRACT

This paper presents a detailed analysis of the CMOS short-circuit power dissipation, on the basis of an elementary CMOS inverter. Accurate, analytical expressions for the inverter output response to an input ramp are derived, which result to an improved formula for the calculation of the short-circuit power dissipation. This improvement is due to the fact that the new derivations take into account the complete expression of the short-circuit current.

1. INTRODUCTION

Recently, the growing demand for low-power portable communications and computing systems, has elevated the power consumption as one of the most critical parameters in many chip designs [1]. Thus, it is important to precisely estimate the power dissipation during the design phase in order to meet the power specifications without a costly redesign process. Analytical expressions for modeling the power dissipation of basic circuits, in a computationally efficient way, which can be incorporated in switch and logic simulators, are required.

Power dissipation in CMOS circuits consists mainly of two parts, the dynamic and the short-circuit power dissipation. Dynamic dissipation caused by charging/ discharging the capacitive loads is relatively easy to be estimated. Short-circuit power dissipation, which in some designs may be represents a significant percentage (10-20%) of the total dissipation, appears during gate switching when the pull-up and pull-down networks of a CMOS gate are simultaneously ON, resulting in a direct current path between supply and ground. Expressions for describing accurately the short-circuit dissipation even though for simple gates is difficult to be derived. The emphasis of this work is on calculating analytically the short-circuit dissipation of a CMOS inverter. To do this, analytical expressions of the output waveform, for the regions of operation where short-circuit current exists, must be derived. The problem is that an analytical solution of the differential equation describing the inverter operation in these regions, cannot be found and some approximations must be used. The first analytical expressions for the output waveform including the effect of the input slope was presented by Hedenstierna and Jeppson [2], where the influence of the short-circuit current was neglected. These expressions was extended by Kayssi et al. [3] for the case of exponential input waveform, but still only for negligible short-circuit current. More recently in [4], the differential equation describing the discharge of the load capacitor was solved for a rising input ramp considering the currents through both transistors. However, in the case where the NMOS device is saturated and the PMOS device is in the linear region, the quadratic term of the current through the PMOS device was neglected. Vemuru and Thorbjornsen [5] derived an expression for the output waveform, which includes this term of the PMOS current, using a power series to approximate the solution of the differential equation. However, only the first five terms of the series were calculated, and a recursion form for the calculation of higher order terms in order to obtain better accuracy, was not considered.

In this paper, analytical expressions for the output waveform, which overcome the weaknesses of previous works are derived, in order to find a formula for the calculation of the short-circuit dissipation for a CMOS inverter. A simple long-channel, bulk-charge model [6] has been chosen since short-channel models [7] cannot be handled analytically, if the current through both transistors is considered. However, the experience derived from the results using a simple model could be expanded to more advanced models. The first work on the calculation of the short-circuit dissipation of a CMOS inverter was presented in [8] where zero load capacitance, and current waveform which is mirror symmetric about a central vertical axis, were considered. More recently, in [2] a formula for the calculation of the short-circuit energy dissipation without the restrictions of [8] was derived. However, as mentioned above the expression of the output waveform used there, was derived with negligible short-circuit current. Here, it is the first time that a formula for the calculation of the short-circuit power dissipation, which considers the complete expression of the short-circuit current, is introduced.

2. CMOS INVERTER SWITCHING ANALYSIS

The presented analysis is based on the long-channel, bulk-charge transistor model [6]. The derivations presented in the following are for a rising input ramp,

$$V_{in} = \begin{cases} 0, & t \le 0 \\ V_{DD} \cdot (t/\tau), & 0 \le t \le \tau \\ V_{DD}, & t \ge \tau \end{cases} \qquad (1)$$

where τ is the input rise time. However, similar results can be obtained for falling input ramp. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter of Fig. 1, with the assumption that

* Currently on leave of absence from IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA.

0-7803-3073-0/96/$5.00 ©1996 IEEE

there is no gate-drain capacitive coupling, is:

$$C_L \frac{dV_{out}}{dt} = I_p - I_n \qquad (2)$$

Since, short-circuit power is dissipated when the NMOS and PMOS devices are simultaneously ON, we examine the case in which the condition $V_{TN} \le V_{in} \le V_{DD} - |V_{TP}|$ holds for the input voltage, where V_{TN} and V_{TP} are the NMOS and PMOS threshold voltages, respectively. If we consider input ramps such that the NMOS device is still saturated when the input voltage ramp reaches the value $V_{DD} - |V_{TP}|$, which holds for the most practical conditions in VLSI circuits, then there are two different regions of operation for the CMOS inverter. In the following, after normalizing voltages with respect to V_{DD}, i.e. $u_{in} = V_{in}/V_{DD}$, $u_{out} = V_{out}/V_{DD}$, $n = V_{TN}/V_{DD}$, $p = |V_{TP}|/V_{DD}$, and normalizing time with respect to input rise time, $x = t/\tau$, we obtain the differential equations for each region of operation.

Region 1, $n \le x \le x_2$: The NMOS transistor is saturated and the PMOS transistor is in the linear region. x_2 is the normalized time value where the PMOS device enters in the saturation region, i.e. $V_{DS,P} \le (V_{GS,P} + |V_{TP}|)/(1+\delta_p)$, and is determined by the PMOS saturation condition:

$$u_2 = 1 + \frac{x_2 + p - 1}{1+\delta_p},$$

where u_2 is the normalized output voltage value when PMOS device saturates. The differential equation (2), using the current equations of the long-channel, bulk-charge transistor model [6], becomes:

$$C_L \frac{du_{out}}{dx} = -\frac{k_N V_{DD}\tau}{2(1+\delta_n)}(x-n)^2 + k_P V_{DD}\tau\left[(x-1+p)(u_{out}-1) - \frac{1+\delta_p}{2}(u_{out}-1)^2\right], \qquad (3)$$

where k_N, k_P are the NMOS and PMOS transistor transconductances, and δ_n, δ_p are the Taylor series expansion coefficients of the bulk charge. The first term of the right part in (3) corresponds to the NMOS saturation current, and the second term corresponds to the PMOS current during its linear region, which is the short-circuit current. The above differential equation is a non-linear Riccati equation [9] which cannot be solved analytically, if a particular solution is not known. Thus, a power-series expansion method based on [10] has been used, resulting to the following recursive expression:

$$u_{out} = 1 - \sum_{k=3}^{\infty} f_k (x-n)^k \qquad (4)$$

where, $f_2 = 0$, $f_3 = \dfrac{k_N V_{DD}\tau}{6C_L(1+\delta_n)}$,

$$f_k = \frac{A_p}{k}\left[f_{k-2} - (1-p-n)f_{k-1}\right], \quad \text{for } 3 < k \le 6$$

and,

$$f_k = \frac{A_p}{k}\left\{\left[f_{k-2} - (1-p-n)f_{k-1}\right] + \frac{(1+\delta_p)}{2}\sum_{i=3}^{k-4} f_i f_{k-i-1}\right\}, \quad \text{for } k > 6$$

where, $A_p = \dfrac{k_P V_{DD}\tau}{C_L}$.

The power-series expansion of equation (4) is used for small values of A_p ($A_p \le 10$), which covers the most practical cases in VLSI circuits. The second term in the braces for the case of $k>6$ corresponds to the influence of the quadratic current term of the PMOS device which was neglected in [4]. This is inserted to the output waveform after the sixth order coefficient. For the calculation of the short-circuit energy dissipation in [2], an expression of the output waveform with negligible short-circuit current was used. However, it can be observed in Fig. 2 that the influence of the PMOS current, which is included in expression (4), results in a significant voltage difference at the output node of the CMOS inverter.

Region 2, $x_2 \le x \le 1-p$: Both transistors are saturated. In this region, the differential equation (2) becomes:

$$C_L \frac{du_{out}}{dx} = -\frac{k_N V_{DD}\tau}{2(1+\delta_n)}(x-n)^2 + \frac{k_P V_{DD}\tau}{2(1+\delta_p)}(x-1+p)^2, \qquad (5)$$

where the two terms of the right part are the NMOS and PMOS saturation current respectively, as given from the current equations of the long-channel, bulk-charge transistor model. The analytical solution of the above differential equation is:

$$u_{out} = c - \frac{k_N V_{DD}\tau}{6C_L(1+\delta_n)}(x-n)^3 + \frac{k_P V_{DD}\tau}{6C_L(1+\delta_p)}(x-1+p)^3, \qquad (6)$$

where the integration constant c, which is inserted to ensure continuity with respect to region 1, is given by:

$$c = u_2 + \frac{k_N V_{DD}\tau}{6C_L(1+\delta_n)}(x_2-n)^3 - \frac{k_P V_{DD}\tau}{6C_L(1+\delta_p)}(x_2-1+p)^3, \qquad (7)$$

where (u_2, x_2) is the starting point of region 2.

3. CMOS SHORT-CIRCUIT POWER DISSIPATION

It is known that the short-circuit energy dissipation per transition, is given by [2],[8]:

$$E_{SC} = V_{DD}\int I_{SC}\,dt = V_{DD}\int I_p\,dt \,. \qquad (8)$$

The application of the Kirchoff's current law to the output node of the CMOS inverter (Fig. 1) yields:

$$I_p = I_n - I_{C_L} = \frac{k_N V_{DD}^2}{2(1+\delta_n)}(x-n)^2 + \frac{V_{DD}C_L}{\tau}\frac{du_{out}}{dx}. \qquad (9)$$

The short-circuit energy dissipation per transition may then be written as:

$$E_{SC} = \frac{k_N V_{DD}^3\tau}{2(1+\delta_n)}\int_n^{1-p}(x-n)^2\,dx + V_{DD}^2 C_L\left(u_{out}[1-p] - u_{out}[n]\right)$$

$$= \frac{k_N V_{DD}^3\tau}{6(1+\delta_n)}(1-p-n)^3 + V_{DD}^2 C_L\left(u_{out}[1-p] - 1\right), \qquad (10)$$

where $u_{out}[1\text{-}p]$ is the value of the normalized output voltage when the inverter leaves region 2 (then $x=1\text{-}p$), and $u_{out}[n]=1$ as it is the normalized output voltage for $V_{in}=V_{TN}$. Using equations (6) and (10) the short-circuit energy dissipation per transition is written as:

$$E_{SC} = \frac{k_N V_{DD}^3 \tau}{6(1+\delta_n)}(1-p-n)^3 + V_{DD}^2 C_L \left[c - \frac{k_N V_{DD} \tau}{6 C_L (1+\delta_n)}(1-p-n)^3 - 1 \right] \quad (11)$$

It can be observed from equation (11) that for the analytical calculation of the short-circuit energy dissipation per transition, the integration constant c, must be determined. To do this, it is clearly from equation (7) that the calculation of the values x_2, u_2 is required. These values satisfy the PMOS saturation condition, expressed by equation (12), as it has already been mentioned,

$$u_{out} = 1 + \frac{x + p - 1}{1+\delta_p} , \quad (12)$$

and they can be found by solving the system of equations (4) and (12). Since, the order of equation (4) is high, the system of equations cannot be solved analytically. Hence, in the following an approximation for the calculation of x_2, u_2 is introduced, which is illustrated in Fig. 3.

The analytical solution of the differential equation (3), if negligible PMOS current is assumed, is:

$$u_{out} = 1 - \frac{k_N V_{DD} \tau}{6 C_L (1+\delta_n)}(x-n)^3 = 1 - f_3 (x-n)^3 \quad (13)$$

From equations (12), (13) the normalized time x'_2 in which the inverter entered region 2, with the assumption of negligible PMOS current, is derived:

$$x'_2 = \frac{n - (2/3)^{1/3}}{\sqrt{D}\ E^{1/3}} + \frac{E^{1/3}}{18^{1/3}\sqrt{D}} , \quad (14)$$

where, $E = \sqrt{12 + 81 D (n+p-1)^2} + 9\sqrt{D}(1-p-n)$,

and $D = (1+\delta_p) f_3$.

The next step of our approximation is to determine the tangent of the output waveform expressed by (4), at the point which corresponds to x'_2 (see Fig. 3). This tangent is expressed by the following equation:

$$u_{out} = a\,x + b , \quad (15)$$

where, $a = \frac{du_{out}}{dx}(x'_2) = -\sum_{k=3}^{\infty} k f_k (x'_2 - n)^{k-1}$,

and, $b = 1 - a\,x'_2 - \sum_{k=3}^{\infty} f_k (x'_2 - n)^k$.

From equations (12) and (15) an accurate approximation for x_2 is derived:

$$x_2 = \frac{(1+\delta_p) b - \delta_p - p}{1 - a(1+\delta_p)} . \quad (16)$$

By substituting x_2 in equation (4) the normalized output voltage u_2 is calculated. After the calculation of x_2, u_2, a formula for the calculation of the short-circuit power dissipation (P_{SC}) of a CMOS inverter can be derived. Using equation (11) P_{SC} is written as:

$$P_{SC} = 2 f_{CLK} E_{SC} = \frac{k_N V_{DD}^3 f_{CLK} \tau}{3(1+\delta_n)}(1-p-n)^3 + 2 V_{DD}^2 C_L f_{CLK} \left[c - \frac{k_N V_{DD} \tau}{6 C_L (1+\delta_n)}(1-p-n)^3 - 1 \right] , \quad (17)$$

where f_{CLK} is the switching frequency. The factor 2 in (17) comes from the fact that the short-circuit current flows twice per one switching cycle (a switching cycle is two logic level transitions, high-to-low and low-to-high). This, of course, holds for symmetrical inverter, i.e. $k_N = k_P$ and $n = p$. Note, that the error introduced by our approximation of the values x_2, u_2, in the calculation of the short-circuit power dissipation for $k = 16$, is from 0.05×10^{-6} % (for $A_p = 1.5$) to 0.03 % (for $A_p = 9.5$).

The short-circuit energy dissipation percentage of the capacitive energy dissipation per transition, is plotted as a function of A_p in Fig.4. The solid curve, noted as "analytical (2)", has been derived using equation (11), for $n = p = 0.17$, $k_N = k_P = 0.3\ mA/V^2$, and $\delta_n = \delta_p = 0.2$ in order to achieve symmetric falling and rising output waveforms. The dashed curve (analytical (1)) has been derived using the formula for the calculation of the short-circuit energy dissipation proposed in [2], where negligible short-circuit current is assumed in the expression of the output waveform. It can be observed, that the presented approach gives results closer to those derived from long-channel level 3 SPICE simulations (curve with symbols), thus it is more accurate from the previous approach of [2].

4. CONCLUSION

In this paper an improved formula for the calculation of the short-circuit power dissipation in a CMOS inverter, has been derived. In order to achieve that, analytical expressions of the CMOS inverter output ramp response, for the operation regions where short-circuit power is dissipated, have been derived. These expressions take into account the complete form of the short-circuit current. Finally, it has been shown that the proposed formula for the calculation of the CMOS short-circuit power dissipation, gives more accurate results than those of previous works.

REFERENCES

[1] A.P. Chandrakasan, S. Sheng, and R.W. Brodersen, "Low-Power CMOS Digital Design", *IEEE J. Solid-State Circuits*, vol. 27, pp. 473-484, April 1992.

[2] N. Hedenstierna and K.O. Jeppson, "CMOS Circuit Speed and Buffer Optimization", *IEEE Trans. Computer-Aided Design*, vol. 6, pp. 270-281, March 1987.

[3] A.I. Kayssi, K.A. Sakallah and T.M. Burks, "Analytical Transient Response of CMOS Inverters", *IEEE Trans. Circuits and Systems-I*, vol. 39, pp. 42-45, January 1992.

[4] K.O. Jeppson, "Modeling the Influence of the Transistor Gain Ratio and the Input-to-Output Coupling Capacitance on the CMOS Inverter Delay", *IEEE J. Solid-State Circuits*, vol. 29, pp. 646-654, June 1994.

[5] S.R. Vemuru and A.R. Thorbjornsen, "A Model for Delay Evaluation of a CMOS inverter", in *Proc. of ISCAS*, vol. 1, pp. 89-92, May 1990.

[6] J. P. Uyemura, *Circuit Design for CMOS VLSI*. Kluwer Academic Publishers, MA, 1992, pp. 33-34.

[7] T. Sakurai, A.R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas", *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584-594, April 1990.

[8] H.J.M. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits", *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 468-473, August 1984.

[9] H.T. Davis, *Introduction to Nonlinear Differential and Integral Equations*. Dover Publications, NY, 1962, pp. 57-78.

[10] M. Shoji, *CMOS Digital Circuit Technology*. Prentice-Hall, Englewood Cliffs, NJ, 1987, pp. 121-123.

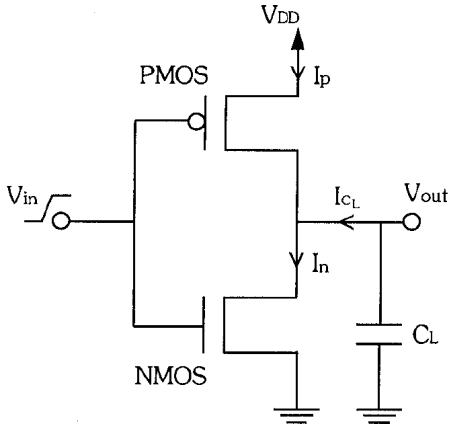

Fig. 1: The CMOS Inverter.

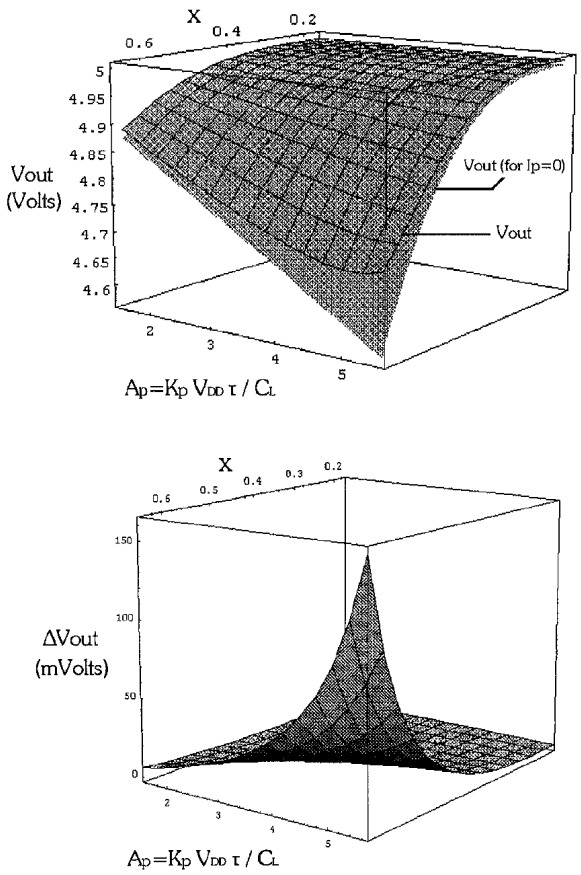

Fig. 2: Difference between the output voltage waveform expressed by equation (4) and that where negligible short-circuit current is assumed, in region 1.

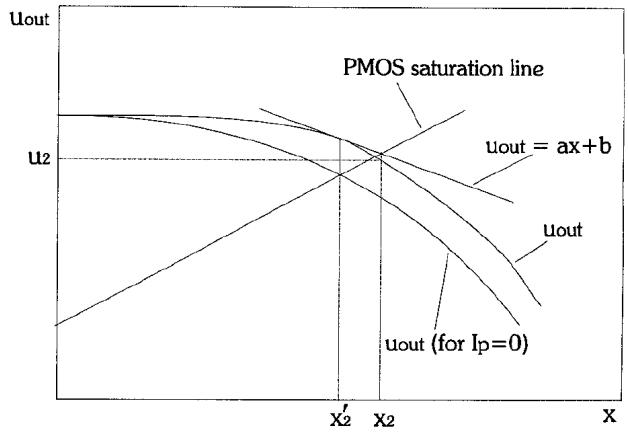

Fig. 3: Approximation of the normalized time x_2, in which the inverter entered region 2.

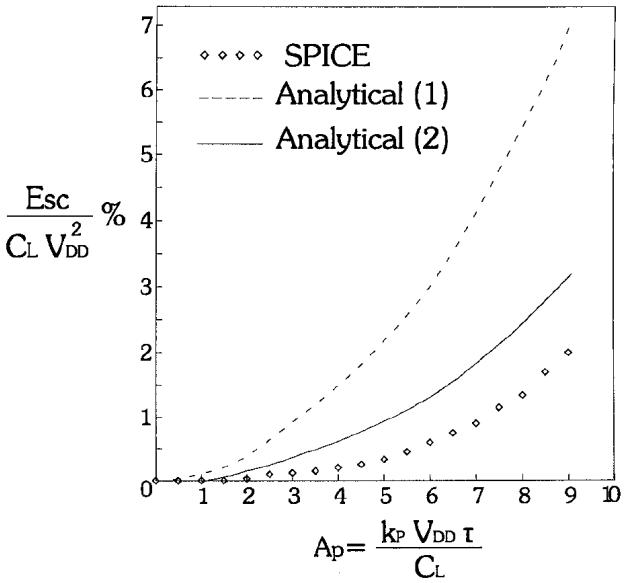

Fig. 4: Comparison between the short-circuit energy dissipation percentage of the capacitive energy dissipation, derived from SPICE and those derived from analytical expressions.