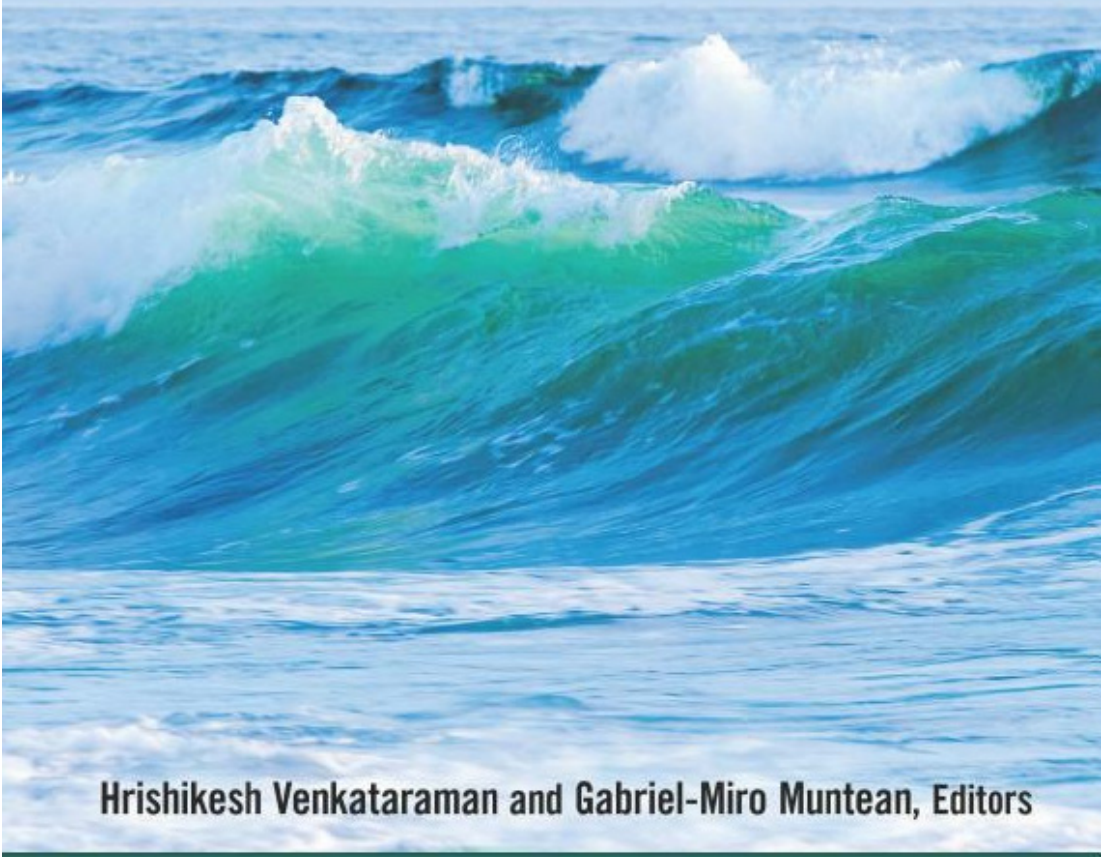
Green Mobile Devices and Networks

Energy Optimization and Scavenging Techniques



Hrishikesh Venkataraman and Gabriel-Miro Muntean, Editors

CRC Press
Taylor & Francis Group

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CRC Press
Taylor & Francis Group
Boca Raton London New York

CRC Press is an imprint of the
Taylor & Francis Group, an **informa** business
AN AUERBACH BOOK

CRC Press
Taylor & Francis Group
6000 Broken Sound Parkway NW, Suite 300
Boca Raton, FL 33487-2742

Version Date: 20111020

International Standard Book Number-13: 978-1-4398-5990-2 (eBook - PDF)

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Contents

SECTION II SCAVENGING TECHNIQUES

Preface

Wireless communications are evolving rapidly toward "beyond 3rd generation (B3G) and 4G systems." At the same time, multimedia transmissions, video-on-demand, gaming, etc. are becoming increasingly popular among the growing number of users. Additionally, over the past couple of years, the demand for multimedia communications and, particularly, video streaming to handheld mobile devices has grown by leaps and bounds. In particular, it is expected that by 2013, mobile phones and other browser-enabled mobile devices will overtake PCs as the most common access device worldwide. As the technology progresses, wireless devices, such as smartphones, iPhones, PDAs, etc., are offering a large number of sought-after features to customers and support for increasingly complex applications. With each passing year, the functionality and computing power of mobile devices is increasing exponentially, with more and more applications and communication technologies being added consistently to handheld wireless devices. The data rate required for supporting these services is also increasing significantly. This implies a high power requirement at the transmitting and, especially, the receiving wireless devices. However, there is an annual power improvement of only 6 percent over past years and this has not grown in tune with processing and communication technologies. This has a serious impact on the practical use of the mobile devices, especially when accessing rich media-based services. For example, the battery of an iPhone 4GS lasts a mere five hours during Internet connectivity on a 3G network.

Given the stringent requirements and the current limitations of the battery powering of mobile devices, serious efforts are required not only to improve the battery quality, but also improve the battery life. In order to achieve greater success from mobile technology over the next decades, the concept of battery recharging every one to two days has to be completely revamped. This is, of course, easier said than done. A very important question that needs to be investigated and would challenge the researchers/handset manufacturers/network operators is what kind of improvement in the battery can be achieved without significantly altering the overall performance? This is a very interesting yet a very difficult proposition. Recently, there have been several efforts to optimize the energy consumption in both devices and networks. At the level of a device receiving video

content via wireless networks, the content's bit rate, frame rate, and color depth could be altered seamlessly depending on the current battery power status. Such a periodic yet a dynamic adaptive mechanism would significantly optimize the battery consumption. An important thing to ponder is that energy optimization schemes can only reduce the consumption and thereby, increase the battery life by a certain but limited amount. There should be alternate mechanisms that need to be used or proposed in order to improve the self reliance of the devices or at least significantly extend the power in the devices by generating or harvesting energy from the environment. An interesting, but challenging aspect is to look at different energy-harvesting techniques and their adaptability to be used by wireless/mobile devices and networks. In order to achieve this, significant changes have to be made in both the hardware mechanisms and software policies to adapt energy use to user requirements for the tasks at hand and to enable automatic recharge from the environment.

Significantly, at the heart of all the technology platforms and handsets introduced are networking and radio communications, thereby enabling base stations/routers/devices to support rich media services, regardless of where the users are physically located. With the latest extensive demand for high-speed Internet browsing and multimedia transmissions over the wireless networks, the focus of mobile networking has been mainly on increasing the data rate and, importantly, the system processing capacity. However, recently it has become quite evident that data rate increase and throughput maximization are not the only objectives in the next generation of wireless systems. *Tomorrow's networks should be optimized for performance and for energy efficiency as well*. A network optimized for both performance and energy implies a very different design and architecture and this is what is needed for high data rate communication to be sustainable in the future. To dramatically reduce the energy consumption of today's wireless networks, a radical new approach needs to be initiated. Hence, the next wave of energy efficient networks will not come simply from more traditional research on single aspects, such as physical layer research, but will require *holistic, system-wide, breakthrough thinking that challenges basic assumptions.*

Harvesting energy from the environment is an important aspect that can create a significant impact in the working pattern of current wireless networks. Energy harvesting can be done at the transmitters, receivers, routers, etc. However, energy harvesting in networks/base stations, etc. is still in a very nascent stage, as compared to energy harvesting in devices. This is primarily because of two reasons. Firstly, the amount of energy required by the wireless networks is very high and it is not possible to harvest such a large amount of energy at the moment. Secondly, the networks/base stations are located at one place and operated by mobile network operators, which are run by big companies. Hence, it becomes easier to power the base station through the existing electricity grid rather than harvesting energy from the environment. However, at the same time, given the

increasing computational complexity and the power requirement of the base stations, extracting energy from the environment to power the operations of the base stations is an extremely relevant issue in the decades to come. In fact, in the sensor network domain, given the critical power requirement, energy harvesting for wireless sensor networks is already being carried out. It is an interesting research challenge to extrapolate the energy-harvesting mechanisms from sensor networks to wireless cellular networks.

Energy harvesting in devices is a relatively easy challenge. This is primarily because of the low power requirement of wireless devices. Further, a wireless device is exposed to different sources of energy in the environment, such as heat, light, mechanical keys, electromagnetic waves, audio, etc. Hence, a holistic approach would be to optimize energy harvesting through each individual mechanism and then integrate these different aspects.

This book is a first of its kind focusing solely on energy management in mobile devices and networks. It provides a detailed insight into the different energy optimization techniques and energy harvesting mechanisms in both wireless devices and networks. A unique aspect of the book is the detailed and integrated coverage of different optimization and energy scavenging techniques by different experts. This has not been dealt with before and offers a unique platform for the readers. The book is divided into two parts. The first part describes various energy optimization techniques, whereas the second part presents the energy-harvesting mechanisms.

The first part has seven chapters that focus on energy optimization techniques. Of these, the first three chapters focus on "energy optimizations in devices," while the next four chapters deal with "energy optimization in wireless networks." Chapter 1 talks about energy management and energy optimization techniques for location-based services in mobile devices. Chapter 2 explains the mechanism for energy efficient supply for mobile devices. Chapter 3 models the energy costs of different applications in wireless devices/handsets and is an extension of their previous proposed work in the same domain. In case of wireless networks, the energy consumption for the components across different wireless networks remain the same. However, the pattern of the energy consumption varies across different types of networks. Given the importance of voice communication in cellular networks, Chapter 4 talks about exploiting on–off characteristics of human speech for energy conservation in WiMAX-based systems. Further, given the amount of voice over Internet protocol (VoIP) IP services, Chapter 5 provides an insight into the quality of experience-based energy conservation techniques for VoIP services in Wireless LAN. Notably, a distributed ad hoc network represents a highly complex network in terms of both implementation and deployment. Hence, Chapter 6 explains the importance of considering multiple criteria (minimum energy, multiple relay, etc.) in a mobile ad hoc network and extends their previous work in this field. Above all, given the amount of energy optimization techniques already developed for wireless

sensor networks, Chapter 7 provides a comprehensive overview of energy optimization in wireless sensor networks and how it could be potentially extrapolated for a generic wireless network.

The second part of the book includes six chapters that focus on energy harvesting techniques. Given the importance and the amount of research work being carried out for energy harvesting in wireless devices, four out of the six chapters in this section are dedicated to factors and mechanisms for different energy harvesting solutions for wireless devices. The last two chapters talk about common energy harvesting techniques in wireless networks. Chapter 8 evaluates CMOS RF- DC rectifiers for electromagnetic energy harvesting in mobile devices. Further, Chapter 9 explains in detail energy scavenging techniques using a magneto inductive method, while Chapter 10 discusses the mixed signal low power techniques in energy harvesting systems. In Chapter 11, we look at designing wireless sensors with intelligent energy-aware middleware and how could this be extrapolated into futuristic wireless devices. Similarly, the last two chapters of the book, Chapter 12 and Chapter 13, provide an energy consumption profile for energy harvested wireless sensor networks and radio frequency energy harvesting/management for wireless sensor networks, respectively.

Green Mobile Devices and Networks: Energy Optimization and Scavenging Techniques can serve as a benchmark for postgraduates, future engineers, and designers in developing energy-optimal solutions and at the same time provide a deeper insight for the next generation of researchers to harvest energy from the environment for developing the next generation telecommunication systems.

The editors would like to wish the audience a happy reading time and would be happy to receive any queries from the readers.

Hrishikesh Venkataraman
Gabriel-Miro Muntean

The Editors

Hrishikesh Venkataraman, PhD, is a senior researcher and Enterprise Ireland (EI) principal investigator with Performance Engineering Laboratory at the Irish national research center—The RINCE Institute, at Dublin City University (DCU), Ireland. He obtained his PhD from Jacobs University Bremen, Germany, in 2007, for his research on wireless cellular networks. He obtained his master's degree from Indian Institute of Technology (IIT) in Kanpur, India, in 2004, and did his master's thesis from Vodafone Chair for Mobile Communications, Technical University Dresden, Germany, in 2003–2004 under the Indo-German DAAD (*Deutscher Akademischer Austausch Dienst*) Fellowship. His research interests include mobile multimedia, wireless communications, and energy in wireless. Dr. Venkataraman has published more than 30 papers in journals, international conferences, and book chapters, and has won a Best Paper Award at an international conference at the University of Berkeley, California, in October 2009. Currently, Dr. Venkataraman is an executive editor of *European Transactions on Telecommunications* (*ETT*) and is a founding member of the UKRI (United Kingdom/Republic of Ireland) chapter of the IEEE (Institute of Electrical and Electronics Engineers) Vehicular Technology Society.

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Chapter 10

Mixed-Signal, Low-Power Techniques in Energy Harvesting Systems

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Contents

10.1 Introduction

Energy harvesting systems pose a new challenge in the domain of circuit design because they must operate with an extremely low-power budget. As is evident, a circuit functioning in such an energy-starving environment must be operated near the fundamental low-power limits and should be designed on the basis of very strict guidelines conforming to the most recent advances in low-voltage and low-power design.

Modern portable systems, which are the main application field of energy harvesting techniques, are mainly mixed-signal systems comprised of a digital core including, amongst others, a central processing unit (CPU) or digital signal processing (DSP) and memory, often surrounded by several analog interface blocks, such as I/O (input/output), D/A (digital-to-analog), and A/D (analog-to-digital) converters, RF (radio frequency) front ends, and more. Therefore, a mobile device is a characteristic example of a mixed-signal system, which is, namely, a system that combines, to some extent, analog and digital circuitry.

The evolution in complementary metal oxide semiconductor (CMOS) technology, which is the dominant technology in portable systems, is motivated by the decrease in the price-per-performance factor for digital circuitry in a pace dictated by Moore's Law, the main effect of which is the shrinking of the dimensions (feature size) of the devices. To ensure sufficient lifetime for digital circuitry and to keep power consumption at an acceptable level, this dimension-shrink is accompanied by lowering of nominal supply voltages. While this evolution in CMOS technology is by definition very beneficial for digital circuits, this is not the case for analog circuits. In addition, although low-power techniques for analog and digital circuits have nowadays sufficiently matured, there still remain some fundamental controversies regarding the design of a mixed-signal system that a designer must take under consideration.

The most efficient way to reduce the power consumption of digital circuits is to reduce the supply voltage, since the average power consumption of CMOS digital circuits is proportional to the square of the supply voltage. On the other hand, the reduction of the supply voltage is also mandatory due to dimension shrinking in order to maintain the electric field at an acceptable level.

The rules for analog circuits seem to be different than those applied to digital circuits. This is mainly due to the fact that the power consumption of analog circuits at a given temperature is basically set by the required signal-to-noise ratio (SNR) and the required bandwidth.

A very important technique that seems to bridge the controversies between analog and digital low-power techniques is based on the ability of CMOS transistor devices to work in the *subthreshold region* (*weak inversion*). CMOS transistors functioning in this region exhibit extremely low power consumption, as a result of extremely low operating current densities that are inherent in the subthreshold operation. Subthreshold operation is not suitable for applications where high performance is needed, but seems a very attractive solution in energy harvesting systems where simple systems are generally implemented.

In the rest of this chapter, the particularities of the low-power design in the digital and the analog domain will be analyzed in order for the reader to gain a deeper knowledge of the effects that specific design choices have on the power performance in the analog and the digital world. In addition, new design techniques will be analyzed and discussed that bridge the analog and digital world controversies toward a successful, mixed-signal, ultralow-power design, suitable for use in an energy harvesting application. Finally, a brief review of the power-aware electronic design automation (EDA) software tools available in the market will be conducted in order to give to the reader a brief guide of the available means for analog and digital low-power design.

10.2 Mixed-Signal Environment in Energy Harvesting Systems

Typical applications of energy harvesting systems are small, wireless autonomous devices, like those used in wireless microsensor networks and radio frequency identification Systems (RFIDs). These types of applications would benefit from unbounded lifetimes in an environment where changing batteries is impractical or impossible, since the concept of energy harvesting involves converting ambient energy from the environment into electrical energy to power the circuits or to recharge a battery. Microsensor nodes must keep average power consumption in the 10 to 100 μW range to enable energy harvesting [1]–[3]. Combining energy harvesting techniques with some form of energy storage can theoretically extend system lifetimes indefinitely. Clearly, this type of system will be much more effective when coupled with the significant power and energy savings made possible by applying power reduction design techniques to their individual components.

10.2.1 Microsensor Wireless Networks

A microsensor node refers to a system that provides sensing, computation, and communication functionality. The block diagram of a typical microsensor node is shown in Figure 10.1. Wireless microsensor networks consists of tens to thousands of distributed nodes that sense and process data and relay the results to the end

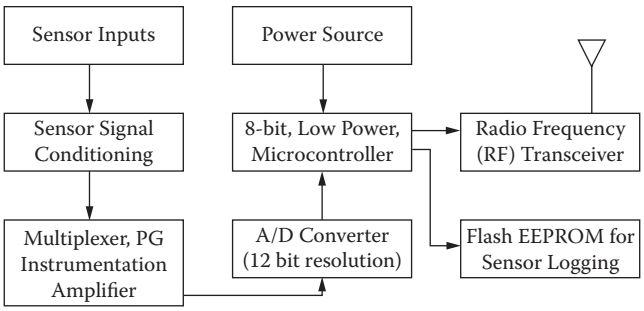

Figure 10.1 A block diagram of a typical wireless microsensor node.

user. Proposed applications for microsensor networks include habitat monitoring, structural health monitoring, and automotive sensing [3] [4].

The performance requirements for microsensor nodes in these applications are very low. The rate at which data changes for environmental or health monitoring, for example, is on the order of seconds to minutes, so the performance achieved even in subthreshold is more than adequate. A very common technique used in microsensor nodes is the duty cycle or shutdown of unused components whenever possible. Although duty cycling helps to extend sensor network lifetimes, it does not remove the energy constraint placed by the power source. Energy harvesting techniques are a necessity in these applications because, if a battery is used instead, it is not possible to recharge or replace batteries frequently. Thus, microsensor networks are a very interesting platform that showcases the need for new low-energy design techniques, which must be applied in the analog and digital domains. This is evident also from Figure 10.1, where a classical mixed-signal system can be easily identified.

10.2.2 Radio Frequency Identification (RFID)

RFID is another typical application that requires extremely low energy consumption [4] [5]. RFID is used to automatically identify objects through RFID tags that are attached to the object. The RFID tag is able to transmit and receive information wirelessly using radio frequencies. An RFID tag contains a limited amount of digital processing logic along with an antenna and communication circuits.

There are two main types of RFID tags. An *active* RFID tag communicates with the reader by transmitting data. Active tags frequently require a power source to supply the energy for transmission, and any extra energy saved due to application of low-power design techniques could be used for extended processing and longer range of communication. A *passive* RFID tag communicates with the reader by modulating the load that the reader sees. This means of communication requires less energy, so passive tags often operate on energy that is converted from the

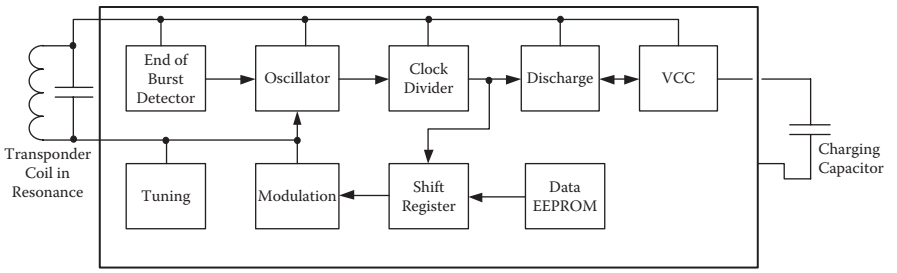

Figure 10.2 Typical block diagram of an RFID tag.

received signal. Passive nodes are usually smaller as a result, and their lifetimes are not limited by energy.

Reducing power consumption and using energy harvesting would benefit both types of tags. This is straightforward for active tags where minimizing the power consumption leads to both increased transmission range and/or longer battery lifetimes. For passive tags, the power is constrained by the ability to utilize the converted energy from the antenna. If the digital logic power dissipation could be reduced and the system could be assisted from an extra energy source, then the distance from the reader to the tag could increase because less transmitted power has to reach the tag.

As is indicated in Figure 10.2, an RFID tag is comprised of several analog and digital parts, which constitute a mixed-signal environment. To this end, if true low power is to be achieved, the reduction of power consumption of analog and digital parts of the system must be addressed.

10.3 Low Power Techniques in Digital Design

Average power consumption in digital CMOS circuits is more important than peak power as instances of peak power consumption when all the circuit components are on is rare. Ideally, CMOS gates consume power when the output node makes a switching transition. However, there are short circuit and leakage currents through the device that result in wasteful power dissipation. The average power P_{avg} consumed by a CMOS circuit can be represented mathematically as:

$$\begin{aligned} P_{avg} &= P_{switch} + P_{ShortCkt} + P_{lkg} \\ &= (C_L \cdot V_{SWING} \cdot V_{DD} \cdot f_{CLK} \cdot \alpha) + (I_{ShortCkt} \cdot V_{DD}) + (I_{lkg} \cdot V_{DD}) \end{aligned} \tag{10.1}$$

The first term on the right-hand side of equation (10.1), i.e., switching power P_{switch}, represents the power consumed by the switching capacitance or load

capacitance C_L of the CMOS circuit. This is the power consumed in charging the load capacitance when the device makes a 0 to 1 transition. It represents approximately 60 to 70 percent [1] of total power consumed. Besides C_L, switching power is also a function of the supply voltage V_{DD}, the voltage difference between logic 1 and logic 0 V_{SWING}, the clock frequency f_{CLK}, and the node transition activity factor α. V_{SWING} usually equals the supply voltage V_{DD}, but for internal nodes, it could be less than V_{DD}.

The second term of equation (10.1), the short circuit power $P_{ShortCkt}$, refers to the power dissipated due to the direct path short circuit current $I_{ShortCkt}$, through the PMOS (p-type MOS) and NMOS (n-type MOS) transistors of static logic circuits during a switching transition. It accounts for 20 percent of total power dissipated in static circuits as there is no short circuit current for dynamic design because of precharging. The short circuit current is a function of the rise and fall time of the input and output signals, amount of capacitive load, size of the CMOS devices, and the gate capacitance, especially the equivalent gate to drain capacitance [6].

The last term in equation (10.1) corresponds to power dissipated due to leakage current I_{lkg}. Usually, leakage current accounts for approximately 2 to 3 percent of the total power. Though, ideally, no power is consumed when both PMOS and NMOS transistors are off, power due to I_{lkg} arises from inherent reverse biased diode currents I_{lkg} and subthreshold effects I_{subtkg} of the transistors. The leakage current is strongly a function of the fabrication technology.

Although power consumption is generally considered as a term identical to that of energy consumption, it is worthwhile to notice a fundamental difference in the case of digital circuits. The power consumed by a device is by definition the energy consumed by unit time. In other words, the energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T_{op}), hence:

$$E = \int_0^{T_{op}} P(t)\,dt \tag{10.2}$$

If we substitute $P(t)$ in equation (10.2) by the switching power of a digital circuit, which is the main component of the total power consumption P_{switch} and we assume that an operation requires n clock cycles, T_{op} can be expressed as n/f and so we get:

$$E = n \cdot C_L \cdot V_{SWING} \cdot V_{DD} \cdot \alpha \tag{10.3}$$

It is important to note that the energy per operation is independent of the clock frequency. Reducing the frequency will lower the power consumption, but will not change the energy required to perform a given operation. Since the energy

consumption is what determines the battery life, it is imperative to reduce the energy rather than just the power. It is, however, important to notice that the power is critical for heat dissipation considerations.

10.3.1 Reducing Power in Digital Circuits

Because switching power accounts for the major portion of the power consumed, any attempt at low-power design should try to minimize it. To this end, low-power design methodologies [7] [8] at every level should aim at reducing the variables in that term, namely, C_L, V_{DD}, V_{swing}, f_{clk}, and a. However, significant reduction of the power consumption can occur through the following interventions:

1. *Supply Voltage V_{DD} Reduction:* Power consumed by a CMOS device is proportional to the square of the supply voltage V_{DD} and, hence, lowering the supply voltage would result in a quadratic reduction in power consumption, though device current reduces only linearly with V_{DD}. It can be proved that in this way the power can be practically reduced by one to eight times [9]. Supply reduction can be achieved through some special circuit manipulations and through feature size scaling, but the designer must be very careful because often these techniques impose serial limitations, such as circuit delay and degraded functional throughput. For computationally intensive functions, one of the effective ways to reduce power consumption while still operating at low voltage is to parallelize the computation by modifying the algorithm and the architecture. The key to architecture-driven voltage scaling is to exploit concurrency (pipelining and parallelism) in execution. Also, the combination of architectural optimization with threshold voltage reduction can scale down supply voltage to the sub-1 V range. To compensate for the loss in speed due to voltage scaling, it is possible to upsize the transistors that are in the critical delay path, or by transistor sizing, using fast logic structures [10].
2. *V_{swing} Reduction:* Power consumption of a CMOS logic gate with a fixed supply voltage V_{DD} also can be reduced by restricting the voltage swing V_{swing} at the output node [10] [11]. Usually, the output node of the gate will make rail-to-rail transitions (V_{DD} to 0 or 0 to V_{DD}). But, if an NMOS device has been used instead as a pull up, the output will limit the swing to ($V_{DD} - V_T$). The power consumed for a 0 to ($V_{DD} - V_T$) in such a case will be $C_L \cdot V_{DD} \cdot (V_{DD} - V_T)$, and the reduction in power consumption (over a rail-to-rail scheme) is proportional to $V_{DD} / (V_{DD} - V_T)$. However, there are a few drawbacks with such a design, such as the reduced noise margin and increased power consumption at the subsequent stage [12].
3. *Load Capacitance (C_L) Reduction:* An obvious way to reduce the load capacitance is to reduce the CMOS device size since scaling reduces the channel and parasitic capacitance [12]. Logic/circuit minimization through effective partitioning can also reduce the load capacitance.

4. *Node Transition Activity* α *Reduction:* Switching activity reduction can help to reduce power consumption in CMOS devices as power is consumed only during transitions. Various techniques range from simply powering down the complete circuit or portions of it, to more sophisticated schemes in which the clocks are gated or optimized circuit architectures are used that minimize the number of transitions [13]. An important attribute that can be used in circuit and architectural optimization is the correlation in the temporal sequence of data because switching should decrease if the data are slowly changing, i.e., highly positively correlated. Thus, knowledge about signal statistics can be used to reduce the number of transitions. The techniques for a reduction span all levels of the system design from the physical design level, to the logic level where logic minimization and logic level power down are the key techniques to minimize the transition activity [13].

Though switching power accounts for the major share of the total power dissipated, short circuit and leakage power usually amount to 20 to 30 percent. In order to reduce short circuit power, gate capacitances, device size, and the rise and fall time of the signals should be reduced. Leakage power, on the other hand, can be reduced by accurate device modeling and threshold control. The various power-reducing parameters discussed can be optimized at various design levels to a different extent.

10.4 Low Power Techniques in Analog Design

Power is consumed in analog signal processing circuits to maintain the signal energy above the fundamental thermal noise in order to achieve the required signal-to-noise ratio (SNR). A representative figure of merit of different signal processing systems is the power consumed to realize a single pole. The minimum power necessary to realize a single pole can be derived by considering the basic integrator presented in Figure 10.3 where an ideal 100 percent current efficient transconductor is used, in the sense that all the current pulled from the supply voltage is used to charge the integrating capacitor [14].

The power consumed from the supply voltage source V_{DD} that is necessary to create a sinusoidal voltage $V(t)$ across capacitor C having peak-to-peak amplitude V_{PP} and frequency f can be expressed as:

$$P = V_{DD} \cdot fCV_{PP} = fCV_{PP}^2 \cdot \frac{V_{DD}}{V_{PP}} \tag{10.4}$$

and the signal-to-noise ratio is given by:

$$SNR = \frac{V_{PP}^2/8}{kT/C} \tag{10.5}$$

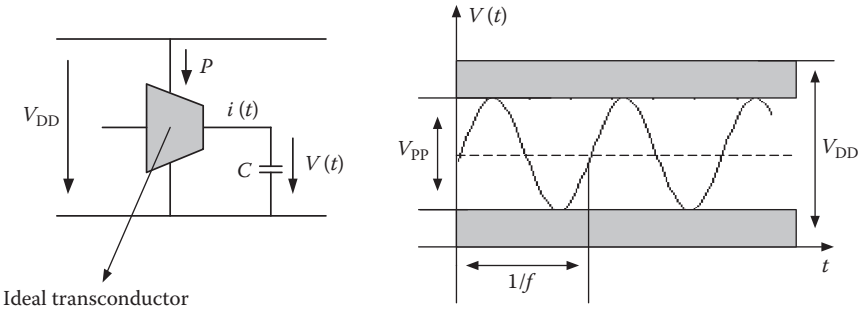

Figure 10.3 An ideal, single-pole analog processing filter.

Combining equation (10.4) and equation (10.5), we get:

$$P = 8kT \cdot f \cdot SNR \cdot \frac{V_{DD}}{V_{PP}} \tag{10.6}$$

According to equation (10.6), the minimum power consumption of analog circuits at a given temperature is basically set by the required SNR and the frequency of operation (or the required bandwidth). Since this minimum power consumption is also proportional to the ratio between the supply voltage and the signal peak-to-peak amplitude, power efficient analog circuits should be designed to maximize the voltage swing. The minimum power per pole for circuits that can handle rail-to-rail signal voltages (V_{PP}= V_{DD}) reduces to [15]–[18]:

$$P_{MIN} = 8kT \cdot f \cdot SNR \tag{10.7}$$

This absolute limit is very steep because it requires a factor 10 of power increase for every 10 dB of signal-to-noise ratio improvement. It applies to each pole of any linear analog filter (continuous and sampled data [19]) and is reached in the case of a simple passive RC (resistor–capacitor) filter, whereas the best existing active filters consume about two orders of magnitude more power per pole. High Q poles in the passband reduce the maximum signal amplitude at other frequencies and, therefore, increase the required power, according to equation (10.6).

Approximately the same result is found for relaxation oscillators, whereas the minimum power required for a voltage amplifier of gain A_v can be proved to be always larger or equal to:

$$P_{MIN} = 8nkT \cdot \Delta f \cdot \mathbf{A}_V \cdot SNR \tag{10.8}$$

which mean that is again proportional to SNR and is $n \times A_v$ times larger than the limit given by equation (10.7).

10.5 Comparison of the Power Consumption of Analog and Digital Circuits

The minimum power for an analog system can be compared to that of a digital system, which, if the transistors are considered ideal, corresponds to the switching component P_{Switch} of equation (10.1), i.e.:

$$\begin{aligned} P_{\min-digital} &= C_L \cdot V_{SWING} \cdot V_{DD} \cdot f_{CLK} \cdot \alpha \\ &= P_{\min-digital} = E_{tr} \cdot f_{CLK} \cdot \alpha \end{aligned} \tag{10.9}$$

In equation (10.9), each elementary operation requires a certain number of binary gate transition cycles, each of which dissipates an amount of energy E_{tr}. Due to the Nyquist theorem, f_{CLK} must be at least twice the signal bandwidth so f_{CLK} can be considered to be the signal bandwidth if we account a factor (1/2) into the constant E_{tr}.

The number m of transitions is only proportional to some power m of the number of bits N, and, therefore, power consumption is only weakly dependent on SNR (essentially logarithmically) [20]:

$$a = N^m \approx [\log(SNR)^m] \tag{10.10}$$

Comparison with analog is obtained by estimating the number α of gate transitions that are required to compute each period of the signal, which for a single pole digital filter can be estimated to be approximately:

$$a \cong 50 \cdot N^2 \tag{10.11}$$

From equation (10.9), $E_{tr} = C_L \cdot V_{SWING} \cdot V_{DD} = C_L \cdot V_{DD}^2$, which varies from 10^{-12} to 10^{-15} Joule.

Combining equation (10.9) to equation (10.11), we get:

$$P_{\min-digital} \cong E_{tr} \cdot f_{CLK} \cdot 50 \cdot [\log(SNR)]^2 \tag{10.12}$$

Therefore, the relationship between switching energy and signal-to-noise ratio (S/N) is logarithmic. Comparison of analog and digital fundamental limits is depicted in Figure 10.4, and clearly shows that analog systems may consume much less power than their digital counterparts, provided a small signal-to-noise ratio is acceptable. But, for systems requiring large signal-to-noise ratios, analog becomes very power-inefficient.

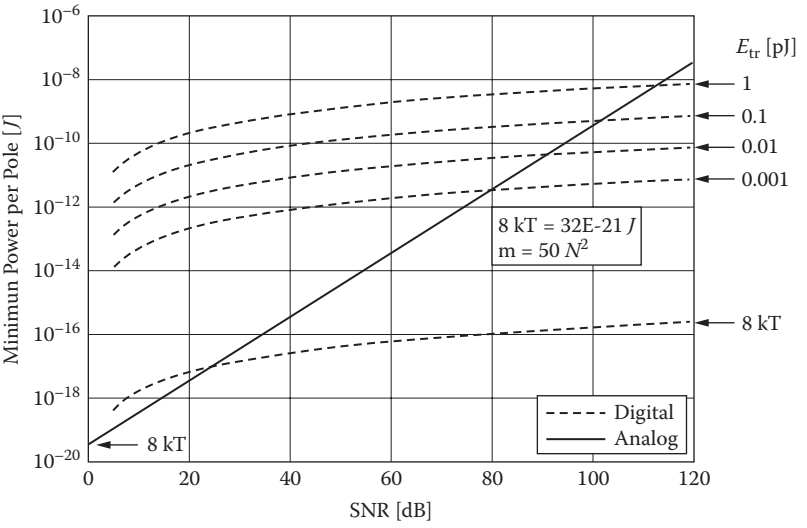

Figure 10.4 Minimum power consumption of analog and digital circuits.

10.6 Combination of Techniques Toward Low-Voltage, Mixed-Signal Design

Unlike digital circuits where, according to equation (10.3), the power consumption decreases with the square of the supply voltage, reducing the supply voltage of analog circuits while preserving the same bandwidth and SNR has no fundamental effect on their minimum power consumption. However, this absolute limit was obtained by neglecting the possible limitation of bandwidth BW due to the limited transconductance g_m of the active device. The maximum value of BW is proportional to g_m/C. Replacing the capacitor value C by g_m/BW in equation (10.5) and expressing the product of the SNR times the bandwidth yields:

$$SNR \cdot BW = \frac{V_{pp}^2 \cdot g_m}{8kT} \tag{10.13}$$

In most of the cases, scaling the supply voltage V_{DD} by a factor K requires a proportional reduction of the signal swing V_{pp}. Maintaining the bandwidth and the SNR, therefore, is only possible if the transconductance g_m is increased by a factor K^2. If the active device is a bipolar transistor (or a MOS transistor biased in subthreshold region), its transconductance can only be increased by increasing the bias current I by the same factor K^2 and, therefore, power $V_{DD} \cdot I$ is also increased by K.

The situation is different if the active device is a MOS transistor biased in strong inversion. Its transconductance can be shown to be proportional to I/V_P, where V_P is the pinch off or saturation voltage of the device. Because this saturation voltage also has to be reduced proportionally with V_{DD}, then increasing g_m by K^2 only requires an increase of current by a factor K and, hence, the power remains unchanged. However, even in this case, supply reduction has serious effects on the functionality of the circuit, since it affects the maximum frequency of operation. For a MOS transistor in strong inversion, the frequency f_{max}, for which the current falls to unity, is given by approximately:

$$f_{\max} = \frac{\mu \cdot V_P}{L^2} \tag{10.14}$$

Therefore, if the process is fixed (channel length L constant), a reduction of V_{DD} and V_P by a factor K causes a proportional reduction of f_{max}.

Reduction of the supply voltage also has an implicit effect on the dynamic range of the analog processor. The *dynamic range* (*DR*) of an ideal integrator, such as this of Figure 10.3, is given by [20]:

$$DR_{\max} = \frac{CV_{DD}^2}{8kT} \tag{10.15}$$

Therefore, implementation of an analog signal processing circuit with a specific dynamic range, in an environment of low-supply voltage, poses an additional challenge for the analog designer.

Unfortunately, in analog systems, low-voltage limitations are not restricted to power or frequency problems. For example, reducing V_P also increases the transconductance-to-current ratio of MOS transistors that, in turn, increases the noise content of current sources, decreasing SNR this way, while at the same time it drastically degrades their precision.

10.7 Optimum Combination of Analog and Digital Low-Power Techniques

As is evident from the above, the main tool that a designer has toward lowering the power consumption of a digital circuit, namely the voltage supply reduction, is not so effective in analog design because power consumption of analog circuits is mainly dependent on SNR, and voltage supply usually leads to an increase of power consumption.

10.7.1 Instantaneous Companding Technique

A possible way to maintain a sufficient dynamic range when reducing the supply voltage, without degrading the power consumption of analog signal processing circuits, is to use the instantaneous companding technique [21]–[23]. In this approach, the currents are compressed when transformed into voltages and expanded when transformed back to currents. The input current has to be predistorted in order to preserve a linear operation.

The basic idea is to ensure that the signal in the channel is always on a level that is significantly over the noise level. To achieve this, the signal is preamplified (predistorted) through amplifier g, but, in order to keep distortion at an acceptable level, it is important not to over-amplify the signal. For this reason, large signals are amplified by a smaller gain than small signals, in a way that amplified signals are always near the maximum dynamic range of the channel. After passing through the channel, signals must be recovered by undergoing the inverse amplification procedure.

As is evident from the above, the gain of the amplifier g depends on the signal level, and, of course, is nonlinear. In instantaneous companding (Figure 10.5), this can be achieved by using nonlinearity, which has small signal gain increases inversely proportional with the signal level, such as that indicated in Figure 10.6.

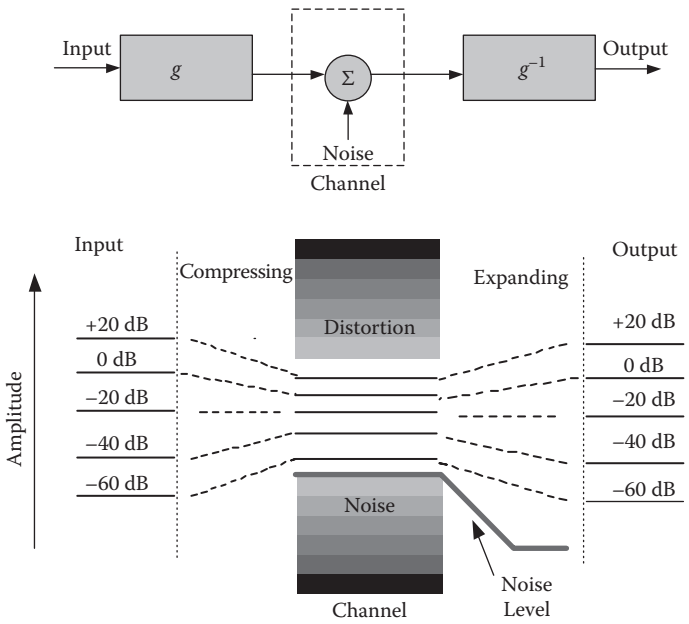

Figure 10.5 The instantaneous companding principle.

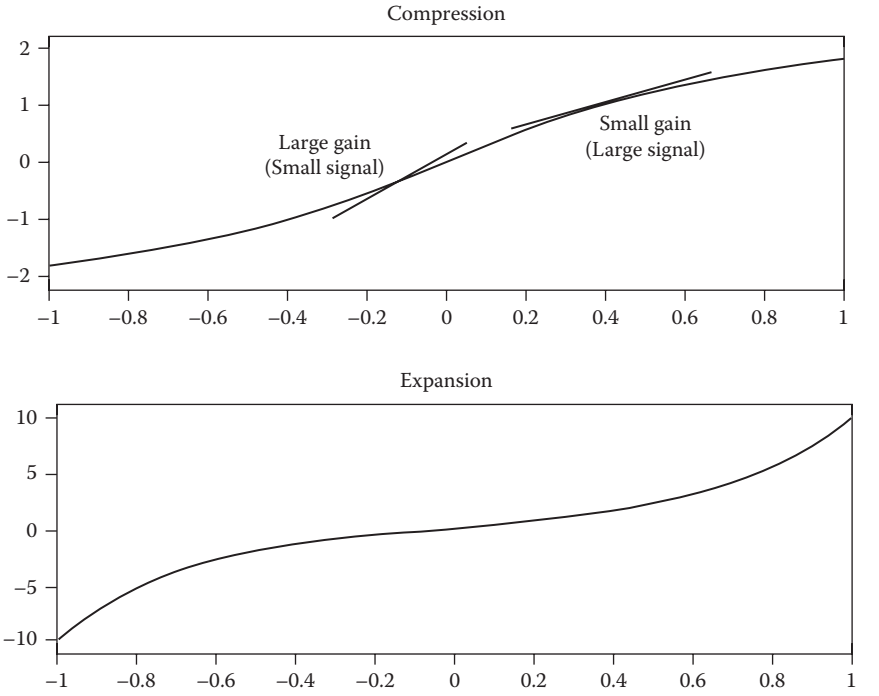

Figure 10.6 Appropriate, signal-dependent shapes for instantaneous companding.

The choice of the amplifying function is not restricted, in theory, but, since the predistortion of the signal requires the derivative of this expanding function, it is much easier to realize it using the exponential function because it is invariant to the differentiation operator and can be implemented either by the current-to-voltage characteristic of a bipolar transistor or a subthreshold-biased MOS transistor.

It can be shown that, for the instantaneous companding circuits, the following statements are valid:

1. SNR is constant and independent of signal level, in contrast to common circuits where SNR depends on signal level.
2. Dynamic range in companding circuits is larger than the maximum SNR, while in common circuits is equal to the SNR.
3. The maximum SNR does not change and, therefore, the power consumption remains unchanged.

Hence, in these circuits, power can be saved if the SNR can be reduced to the minimum required while maintaining the necessary dynamic range.

10.7.2 Subthreshold CMOS Design

A very important technique that seems to bridge the controversies between analog and digital low-power techniques is based on the ability of CMOS transistor devices to work in the subthreshold region (or weak inversion). CMOS transistors functioning in this region exhibit extremely low power consumption as a result of extremely low-operating current densities.

A CMOS transistor is considered to be in a strong inversion region of operation, when the voltage V_{GS} between its gate and source terminals is greater than a threshold voltage V_T. In this region, the drain current I_D of the transistor is considered to have a nonzero value, while for $V_{GS} < V_T$, it is usually considered to have a zero value. However, such an abrupt behavior is certainly not usual in nature, and actually the MOS transistor conducts a very low drain current even when $V_{GS} < V_T$. The main characteristic of this region of operation, which is called *weak inversion* or *subthreshold* region, is the extremely low drain current flow, which corresponds in turn to an extremely low drain current. This behavior is well characterized far into the subthreshold region and varies exponentially rather than quadratically with V_{GS}, according to the relation [24]–[26]:

$$I_D = \frac{W}{L} I_{DO} e^{(V_{GS}-V_T)/(nV_t)} \tag{10.16}$$

where

$$I_{DO} \cong \frac{K'2(nV_t)}{e^2} \tag{10.17}$$

In equation (10.17), K' is the transconductance parameter, $V_t = kT/q = 26\,mV$ is room temperature, and n is a constant between 1 and 2. Typical current densities, for I_D in this region of operation, lie in the pA range. Due to these very low current density levels, weak-inverted CMOSs are convenient for the design of ultra-low power applications.

In this region of operation, CMOS devices exhibit some very interesting features:

- Exponential I–V characteristics of subthreshold MOS devices provide the opportunity to implement analog current-mode circuits with very wide tunability. The possibility to change the bias current in a wide range especially provides appropriate bases to design wide frequency tuning range circuits.
- Exponential I–V behavior of the subthreshold MOS devices makes them suitable to be used for designing for analog log-domain, instantaneous companding circuits.

- CMOS devices in this regime exhibit maximum transconductance (g_m) to bias current (I_{DS}) ratio, i.e., g_m/I_{DS}, which means that the power efficiency of the MOS circuit can be maximized.
- Another very attractive characteristic of subthreshold MOS transistors is their ability to work under very low supply voltage. Therefore, it is possible to reduce the supply voltage of a CMOS inverter down to almost $4V_T$, while preserving sufficient gain for logic operation. Therefore, it is possible to use CMOS logic circuits deeply biased in subthreshold region. This means that if the speed of operation is not the premier design issue, it is possible to reduce the supply voltage and, hence, reduce the power dissipation of a system, which is mostly proportional to the dynamic power consumption.

Emerging new applications, such as energy harvesting systems, which require very low power consumption, has made subthreshold circuits very popular. Subthreshold operation is not suitable for applications where high performance is needed, but seems a very attractive solution in medium (1 Ms–10 Ms) or low (10 Ks–100 \Ks) data throughput systems, where energy consumption and cost are the most important parameters [25].

10.8 Power-Oriented Electronic Design Automation (EDA) Tools

As has been pointed out throughout this chapter, power consumption is a very critical parameter that has to be taken into account during the design of electronic circuits for energy harvesting applications, in order to provide the appropriate energy savings. To facilitate low-power design, electronic design automation (EDA) tools are required, which include efficient methods for fast and accurate estimation of energy dissipation as well as for the design of circuits and systems with certain power consumption constraints [27]–[34].

To date, power-oriented EDA tools have been developed in two main directions:

1. Analysis and modeling
2. Optimization (reduction) of the power consumption of circuits and systems

As shown in Figure 10.7, tools regarding both directions have been developed in several abstraction levels (i.e., level of the input design description), such as transistor level, gate (logic) level, register transfer (RT, architectural) level, and behavioral (algorithmic, system) level [28]-[35]. A netlist of interconnected transistors is at the transistor level, while a netlist of interconnected logic cells is at the logic level. At the register transfer level, designs are described in hardware description languages (e.g., VHDL), and at the behavioral level the

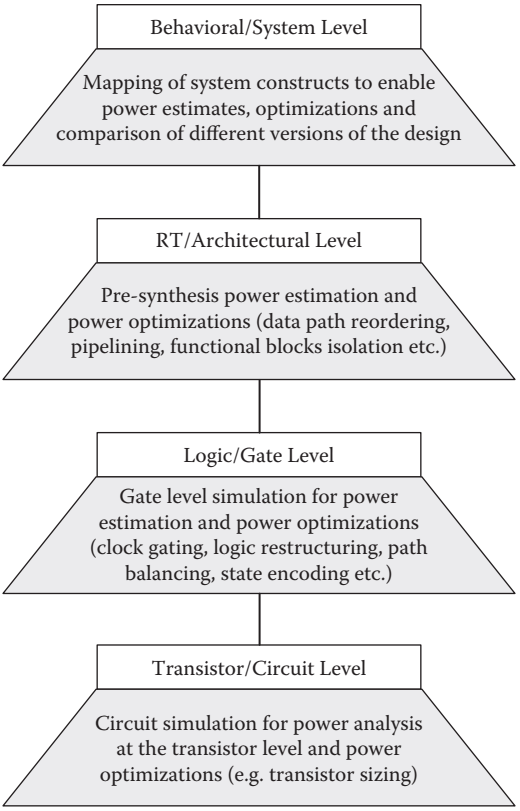

Figure 10.7 Power-oriented design flow with power analysis and optimization steps.

functionality of a design can be described by using hardware description languages (with more abstract functions) or high-level programming languages, such as C, C++, and SystemC.

While the evolution of analysis, synthesis, and optimization EDA tools for digital circuits and systems is fast and satisfactory, the analog portion of design automation has not been able to keep up with its demand. Despite that some efforts have been attempted in this area, there are not yet practical and efficient power-aware analysis and optimization tools that are generally accepted in the analog designers' community [36] [37]. The absence of analog power-aware EDA tools comparable to digital counterpart constitutes a serious bottleneck in designing mixed circuits and systems. Existing analog design automation methodologies are trying to optimize performance and power by using extensive circuit (SPICE-like) simulations based on precise transistor models (e.g., EKV subthreshold model [15]), in order to adjust transistor sizes. An alternative approach is the sizing of

the circuit by using equation-based methods that are based on simplified device equations and approximations. An additional option is the use of analog/mixed-signal languages (AMS-HDL) [38] to speed up mixed-signal current and power simulation. While languages, such as Verilog-AMS and VHDL-AMS, hold a lot of promise, they are only really applicable for full-chip functional verification. They cannot be used for accurate transistor-level power and mixed-signal timing analysis because they cannot accurately model the analog circuitry and device-level effects that can cause leakage.

10.8.1 Transistor Level Tools

Power analysis tools at the transistor level are the most accurate, but also require the most time-consuming analysis. Their run time characteristics in combination with the fact that the whole transistor level description has to be available to the designer before their use limit their applicability to large circuits. Such tools are usually used for creating power models for relatively small elements (characterization) in order to use them at a higher level of abstraction. Transistor level circuit simulators (SPICE-like simulators) can be easily used for circuit power analysis. Their operation is based on detailed equations in order to model the transistors' behavior under various conditions, resulting in limited capacity and analysis speed. An advantage of the use of circuit simulators for power analysis is that they can be applied in either digital, analog, or mixed-signal circuits as well as for transmission line power analysis. An alternative approach to SPICE-like circuit simulators is the power analysis at the switch level that models each transistor as a nonideal switch considering several electrical properties, and leads to significant capacity and run-time improvements.

The process of circuit power characterization is provided by modeling tools that control the circuit simulation engine in order to produce the required power characterization data. These modeling tools use as input the transistor level netlist and the functional description for each cell that needs to be characterized, along with process and operating conditions, such as transition times, output loads, temperature, supply voltage, etc., while at the same time they perform stimulus generation in order to lead the simulation and to produce the power characterization data for each cell.

Power optimization at the transistor level is based on the transistor sizing concept, i.e., employing the smallest transistors to achieve low power while still satisfying the circuit's timing constraints as well as on the transistor reordering concept. The disadvantage of these approaches is that they can be applied only in custom designs. The input in such tools is the transistor netlist and the circuit's timing constraints, and the target is to reduce power consumption in circuit paths with positive timing margins. An additional category of power optimization tools at the transistor level concerns power grid analyzers that report the gradient of voltages along the power rails, as well as the current densities at different points on the power rails, in order to indicate electromigration violations.

Examples of transistor-level power analysis tools are HSPICE [39] by Synopsys, PSPICE [40] by Cadence (circuit simulators), NanoSim [41] by Synopsys (switch-level power analyzer), and SiliconSmart [42] by Magma Design Automation (transistor level modeler). Examples of transistor-level power optimization tools are AMPS [43] and RailMill [44] by Synopsys.

10.8.2 Gate-Level or Logic-Level Tools

In order to improve the speed and the capacity of transistor level tools, logic or gate-level EDA tools have been introduced, which are more compatible with application-specific integrated circuits (ASIC) design flows than transistor-level tools. However, gate-level tools are still limited in capacity and exhibit the disadvantage that they can be applied to a completed design (synthesized and simulated) before meaningful power results can be obtained.

Gate-level power analysis tools compute power consumption per logic element (logic gates, flip-flops, multiplexers, etc.) based on the computation of the nodal activities obtained by logical simulations. Their input is the structural netlist (HDL code) of the design, the power models of the logic elements, as well as the activity information for each logic element produced by logic simulation. The accuracy of gate-level power analysis tools is less than that of transistor-level tools.

Gate-level power optimization tools have been included in logic synthesis tools in order to improve power consumption at the same time as timing and area during the process logic synthesis. These tools search for power-saving opportunities and implement changes, such as clock gating, unit isolation, logic restructuring, path balancing, state encoding, retiming, dual-threshold voltage or dual-supply voltage cell swapping, in order to reduce dynamic as well as leakage power consumption. Reduction of power consumption up to 25 percent can be achieved without violating timing constraints.

An example of gate-level analysis tool is PrimePower [45] by Synopsys, while commercially available power optimization tools at this level are PowerCompiler [46] by Synopsys, and Low Power Solution [47] by Cadence.

10.8.3 Register Transfer-Level Tools

The register transfer (RT) or architectural level is the level of the design hierarchy at which the majority of the system's functional design is performed. Because of that, power analysis and optimization at this level becomes very important. RT-level, power-oriented tools are primarily used as design tools in contrast to gate- and transistor-level tools that are used mainly as verification tools because they can be applied when most of the creative part of the design process is completed. However, in custom circuit design (digital, analog, or mixed-signal), designers should use transistor-level tools for circuit design and characterization.

Architectural-level power estimation tools are less accurate compared to the other two levels defined earlier; however, they help designers make decisions at early stages of the design cycle and provide faster run time. In terms of speed, RT-level tools are about an order of magnitude faster than gate-level tools, which, in turn, are about an order of magnitude faster than transistor-level tools, while in terms of accuracy, RT-level power estimates are 20 percent of actual measurements.

Architectural power analysis tools estimate the power consumption of a design described at the RT level in a hardware description language. The estimation is performed prior to synthesis and the results are linked to the RT-level code to indicate the power contribution of the design portions. The input of power analysis tools at this level is a RT-level code, on which an inferencing procedure is applied that converts the RT-level code into a netlist of instances, such as adders, registers, decoders, and memories. After that, high-level power models are used to estimate the power consumption on an instance-specific basis. Elements not yet present in the design, such as clock distribution and wiring capacitances, are estimated according to specifications produced by subsequent design steps.

Architectural power optimization tools use as input the RT-level description and produce a power-optimized RT-level description. Optimizations, such as clock gating, data path reordering, pipelining, memory restructuring, functional blocks isolation and reduction, data path precomputation, and detection of idle conditions in functional blocks, are implemented.

An example of an RT-level analysis tool is PowerArtist by Apache Design Solutions [48], while commercially available power optimization tools at this level are PowerArtist, PowerCompiler [46] by Synopsys, and Talus PowerPro [49] by Magma Design Automation.

10.8.4 Behavioral-Level Tools and Power Emulation

Behavioral-level power analysis tools are used as input designs in a behavioral hardware description language or in high-level programming languages, such as C, C++, and SystemC. Their distinguishing feature is that the system designer can perform a power analysis at the very beginning of the design process. In addition, since power reduction opportunities are larger at the higher abstraction levels, the ability to evaluate power optimization trade-offs at this level can be very effective. In system level power analysis tools, a mapping between language constructs and hardware objects must be made in order to enable a power estimate. This is achieved by analyzing various combinations of scheduling, allocation, and binding, and then producing power consumption results, along with performance and area estimates.

Behavior-level power optimization is based on the comparison between different versions of the target design, which are analyzed for power in order to select the optimal one. Each of the design versions is mapped onto precharacterized (in terms

of power consumption) objects. Optimizations at this level include rescheduling control and data flow, reducing the number of memory accesses, minimizing overall memory storage requirements, use of different data encodings, power-oriented memory partitioning, and hardware–software mapping.

PowerOpt [50] by ChipVision is a commercially available power analysis tool at the behavioral level, while Atomium [51] developed by IMEC is an example of a behavioral level, power optimization tool.

The increase of circuit sizes and test-bench complexities is straining the capabilities of power estimation tools. Power emulation [52] exploits hardware acceleration to drastically speed up power estimation. The adoption of power emulation is based on the observation that power estimation and analysis is typically performed by evaluating power models for different circuit components, based on the input values seen at each component during circuit simulation, and aggregating the power consumption of individual components to compute the design's power consumption. The functions performed during power estimation and analysis (power model evaluation, aggregation, etc.) can be implemented as hardware components. Therefore, any given design can be enhanced with "power estimation hardware," and mapped onto a prototyping platform (i.e., FPGA-based platform) in order to exercise it with any given test stimuli for obtaining power consumption estimates and supporting power optimization actions.

10.9 Conclusions

In this chapter, the particularities of the low-power design in the digital and the analog domain have been analyzed in order for the reader to gain a deeper knowledge of the effects that specific design choices have on the power performance of circuits in the analog and the digital world. In addition, new design techniques have been discussed that bridge analog and digital world controversies toward a successful, mixed-signal, ultralow-power design, suitable to be used in energy harvesting applications. Finally, the power-oriented EDA tools that are available in the market for the design of low-power analog and digital circuits have been reviewed in order to give the reader a guide to the available means for low-power analog and digital circuits design.

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